A call for papers is now open for the *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* special topic on "Energy-Efficient In-/Near-Memory Computing with Emerging Devices".

Aims and Scope

AI models have continuously shown extraordinary performance in recent years for various applications including computer vision, natural language processing, large language models, etc. Accuracy-driven AI model architectures have largely increased the model sizes and computations at a very fast pace, especially demanding high-density memory storage. Frequent communication between the processing engine and the on-/off-chip memory leads to high energy consumption, which becomes a bottleneck for the AI hardware accelerator design.

To overcome such challenges, in-memory computing (IMC) and near-memory computing (NMC) have been presented as promising schemes for energy-efficient AI acceleration. The weights are stored in the memory cells and dot-product or other operations are performed within or near the memory array. Regarding the memory technologies for the IMC/NMC scheme, SRAM is mature but is volatile, consumes large area (e.g. 8T/10T bitcells) and suffers from the leakage power in the CMOS devices. Such disadvantages promoted the non-volatile memory (NVM) as an attractive solution for area-efficient IMC/NMC-based AI acceleration.

NVMs presented in the literature from both academia and industry include resistive random access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic random access memory (STT-MRAM), ferroelectric field effect memory (FeRAM, FeFET), ferroelectric capacitive device, etc. Notably, the foundry companies including Intel, TSMC, Samsung, and Globalfoundries have commercialized or are prototyping monolithically integrated NVM technologies, e.g. RRAM, MRAM, FeRAM/FeFET, etc.

Compared to SRAM, NVM based IMC/NMC could provide bitcell array density benefits, but the peripheral circuits need to be considered together, and achieving higher energy-efficiency can be challenging due to high current consumption when turning on multiple low-resistance-state devices simultaneously. To address these concerns, new schemes for energy-efficient IMC/NMC with emerging NVM devices are being investigated and developed.

This special topic of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) is in line with such efforts and aims to call for paper submissions on the recent research advances in the area of the energy-efficient in-/near-memory computing spanning devices, circuits, and systems. Papers on the interaction and co-optimization of the materials and devices as well as circuits and architecture are solicited.

Topics of Interest include but are not limited to:
Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of compute-in-memory. Memory technologies of interest include (but not limited to) SRAM, DRAM, eDRAM, NOR/NAND Flash, and emerging NVM devices such as PCM, RRAM/CBRAM, STT-MRAM/SOT-MRAM (or other spintronic memories), FeFET (or other ferroelectric memories), etc. The following topics are specifically solicited:

- New materials and devices that can enable energy-efficient IMC/NMC
- Integration of emerging technologies with silicon for energy-efficient IMC/NMC
- Crossbar array design and array-level demonstration for energy-efficient IMC/NMC
- Peripheral circuit design for energy-efficient IMC/NMC
- Architectural-level design for energy-efficient IMC/NMC
- Algorithms and hardware co-design for energy-efficient IMC/NMC
- Benchmarking simulators for energy-efficient IMC/NMC
- New applications for energy-efficient IMC/NMC beyond AI workloads (e.g. combinatorial optimization, general purpose computing, etc.)

Important Dates
Open for Submission: June 1, 2024
Submission Deadline: September 1, 2024
First Notification: October 1, 2024
Revision Submission: October 15, 2024
Final Decision: November 1, 2024
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Paper submissions must be done through the ScholarOne Manuscripts website:
https://mc.manuscriptcentral.com/jxcdc

Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website (also on the next page).

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