August 2020

Currents

CEDA

IEEE Council on Electronic Design Automation

Call for Papers: IEEE Transactions on Computers

This call for papers is for a special issue on Smart Edge Computing and IoT, organized by Prof. Luca Benini, Prof. Taekwang Jang, Dr. Abbas Rahimi, and Dr. Simone Benatti.

The evolution of the Internet-of-Things (IoT) is changing the nature of edge-computing devices. End-nodes have to support, in-place, an increasing range of functionality: multi-sensory data processing and analysis, complex systems control strategies and, ultimately, artificial intelligence. These new capabilities will enable disruptive innovation in wearable and implantable biomedical devices, autonomous insect-sized drones, autonomous smart environmental sensing, safety-critical real-time applications and structural health monitoring, and more. In this special issue, we are seeking contributions on IoT Smart Edge Computing Architectures, Systems and related hardware-software design approaches.

Topics of interest include, but are not limited to:

- Hardware-software design approaches for smart edge processing
- Heterogeneous systems-on-chip and architecture for energy efficient smart edge processing
- Low-power analog and mixed-signal computing, in-memory computing, in-sensor computing
- Edge machine-learning architectures dealing with sensor and signal variabilities
- Neuro-symbolic, brain- and bio-inspired computing paradigms for edge processing
- IO and peripherals for energy efficient interfaces in edge computing system
- Edge processing for biomedical IoT systems and human machine interaction
- Smart edge IoT devices for structural health monitoring and predictive maintenance
- Real-time and safety-critical smart edge sensors for industrial IoT

Submissions to this special section must represent original material that has been neither submitted to, nor published in, any other journal. Articles should be submitted here by selecting the aforementioned special issue. **The submission deadline is August 30.**

Call for Papers: IEEE JxCDC

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JxCDC), an open access only publication, calls for papers on the Special Topic on Coupled Oscillators for Non- von Neumann Computation. This special issue is organized by Prof. Chris Kim and Prof. Azad Naeemi.

When oscillators are loosely coupled to each other, energy transfer between the individual oscillators causes their frequencies to synchronize. The same principle can be found in real life; for instance, metronomes placed on a floating wooden board, pendulums connected via springs, and internal organs following a circadian rhythm. Depending on the strength and time lag of the coupling medium, the phases of the oscillators settle in a way that minimizes the contentions among the oscillating signals. Recent works have shown that the coupled oscillator's natural ability to evolve to the ground state can be exploited to solve computationally intractable problems, such as graph coloring, max cut, factorization, neural networks, associative memories and pattern recognition. Here, the problems are first mapped to a coupled oscillator network by configuring the coupling weights, and the phase information is read out once the ground state is found. While resolving to the ground state, the network may get stuck in a local minima state, which can be avoided by a concept called annealing where random noise is added during the early exploration phase to help the oscillators break out of a local minima state.

Topics of interest include, but are not limited to:

- Emerging device (e.g. optical, NEMS, ferroelectric, spintronic, phase change) based coupled oscillator systems
- CMOS based coupled oscillator systems
- Variability and reliability effects in coupled oscillator systems

- Probabilistic behavior and operation under noise
- Security properties of coupled oscillator systems
- Weight programming and phase readout techniques
- Annealing techniques for coupled oscillator systems
- Network connectivity and architecture considerations
- Testing, parameter turning, and measurements aspects
- Oscillator Neural Networks (ONNs)
- Associative memories based on oscillators
- Techniques for mapping large problems onto coupled oscillator systems
- Graph embedding algorithms for locally connected coupled oscillator systems
- NP-hard and NP-complete problem case studies
- Comparison with quantum computers and software based approaches (e.g. simulated annealing)
- Literature review and historical trends on coupled oscillator systems.

Submission guidelines and a paper template are provided here. **The submission deadline is September 30.**

Call for Participation: Embedded Systems Week

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of hardware and software design for smart, intelligent and connected computing systems. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), one symposium (NOCS), and several workshops and tutorials, ESWEEK allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research and development.

The registration covers all events at ESWEEK including CASES, CODES+ISSS, EMSOFT, NOCS, keynote, panel, workshops, and tutorials. There will be pre-recorded video presentations and pdf versions of each paper available through Whova. Papers and video presentations will be available two weeks before the conference for participants to comment and post questions. During the conference, there will be live sessions for the journal-track papers where participants can engage with the authors. Registration is $10 USD for IEEE members and $20 USD for non-members. The technical program information is available here. The new format of ESWEEK follows a new timeline. On September 7, papers and pre-recorded video presentations will be online. Questions about papers can be asked through the Whova platform. On September 20-25, ESWEEK Virtual Conference will take place with live sessions including short lightning talks and joined Q&A and discussion.

Call for Papers: IEEE/ACM SLIP^2

The 2020 ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding (SLIP^2) is the 22nd, "rebooted" edition of the System-Level Interconnect Prediction (SLIP) Workshop. As computing systems and applications grapple with a post-Moore, post-CMOS, post-von Neumann future, fundamental interconnect problems and pathfinding challenges have become more critical to address than ever before. For submission info and registration, visit the conference website.

SLIP^2, co-located with ICCAD 2020, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology. The technical goal of the workshop is to identify fundamental problems, and foster new pathfinding of design, analysis, and optimization of interconnect and communication fabrics in electronic systems. A special emphasis is placed this year on predictive system interconnect modeling technologies, and on novel interconnect technologies and architectures for a beyond-Moore era. Additionally, a more interactive, workshop-like tone and format (recalling earlier editions of the SLIP workshop) is a goal for SLIP^2 this year.

Original submissions in the form of regular technical papers, invited sessions (tutorials, panels, special-topic sessions), workshop discussion topics, and posters are welcome. Program content is accepted based on novelty and contributions to the advancement of the field. Accepted technical papers will be published in the ACM and IEEE digital libraries. The abstract and full paper submission deadlines are **September 26** and **October 3**, respectively. For submission info, please visit the conference website.

Find us online at ieee-ceda.org.

***IEEE Embedded Systems Letters* is open for submissions.**
Visit ieee-ceda.org/publication/esl-publication/author-guidelines.

***IEEE Design & Test* is open for submissions.**
Visit https://ieee-ceda.org/publication/ieee-design-test-dt/paper-submission-instructions.

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