May 2018

Currents

IEEE Council on Electronic Design Automation

Enhancing Diversity in EDA

CEDA sponsored the first forum on Advancing Diversity in EDA (DivEDA) at DATE 2018 in Dresden, Germany on March 19. The event was co-organized by Ayse Coskun, Boston University and Eli Bozorgzadeh, University of California, Irvine.

The overarching goal of this new event is to help facilitate women and underrepresented minorities (URM) to advance their careers in academia and industry, and consequently, to help increase diversity in the EDA community. The forum was set up as an interactive medium with the aim to provide practical tips to women and URM on how to succeed and overcome possible hurdles in their career growth. Another major goal of the event was connecting senior and junior researchers to ignite longer term mentoring relationships, leveraged by a "speed mentoring" session towards this end.

Organization of the new DivEDA forum was in part enabled and inspired by the experiences collected from WIE ILC. At the forum, Prof. Ingrid Verbauwhede delivered a keynote on "VLSI Design Methods for Low Power Encryption", where she meshed her research and personal career journey. Other speakers and panelists of the first highly successful edition of the DivEDA forum were as follows: Marilyn Wolf, Nuria Llin, Cristiana Bolchini, Sharon Hu, Mary Jane Irwin, Chengmo Yang, Nele Mentens, and Laura Pozzi.

The DivEDA forum is expected to continue in future editions of DATE and DAC. Stay tuned for future developments!

Madrid Global Brainhack– Spanish Chapter

Answering the next generation of open questions in neuroscience will require vast data sets and complex analytical methods. The purpose of Brainhack is to bridge the data science and neuroscience research communities to advance the progress of brain science research.

Madrid Global Brainhack, organized by the Spanish CEDA Chapter (Madrid, 3-5 May 2018) aims to promote collaborations within Spain and to create an international community of scientists interested in the brain research. The event has also offered educational sessions, like hands-on tutorials on basic tools of open collaboration. Brainhack is great for any level of expertise, this is an occasion to learn new methods, develop new skills, meet new people, and just have fun! The event in Madrid included presentations on ongoing projects of the participants, ideas that could seed future collaborations, and panel discussions. The organization proposed some hacking-challenges, where some of them will be presented to prizes such as MATLAB Online Live Editor Challenge or the National Hackathon of e-Health in June. During the BrainHack, the following coding challenges were proposed: "CNIC-QMENTA Challenge," "Reproduction of results of a paper in machine learning for neuroscience," "Matlab Live Editor Challenge," and "EEG Challenge from the Cajal Institute, can your decode human neural electrophysiological signals?"

IoT Summer School– Georgia Tech

Georgia Tech will hold an IoT Summer School on its Atlanta campus on August 6-10, 2018. Invited speakers from multiple institutions will cover all aspects of Internet-of-Things systems, from devices and networks to data science. The intended audience is young professionals including graduate students and industry professionals. In addition to lectures, participants will engage in networking events and a hands-on session.

IEEE CEDA has sponsored a set of room and board scholarships for workshop attendees. Anyone who wants to be considered for a scholarship should submit two items by June 1, 2018 to wolf@ece.gatech.edu: an email with a one-paragraph description of their interest in the summer school; and a separate email from their research advisor in support of their participation. More information can be found here.

ACM SIGDA University Demonstration

The 30th SIGDA University Demonstration (UD, previously University Booth) will take place at the Design Automation Conference (DAC) on June 26, 2018. UD is an excellent opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially

encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

Participants will be provided with modest travel grant reimbursements. There will be one "University Demo Best Demonstration" award and two "University Demo Best Demonstration, Honorable Mention" awards. Submission is made online until May 08. For further details please visit the ACM SIGDA UD site.

Electronic Design Process Symposium

The Electronic Design Process Symposium (EDPS) is the leading forum for advanced chip and systems development and CAD methodologies. As we approach the end of Moore's law scaling, innovative packaging techniques are becoming increasingly important as package, board, and other system components drive significant cost reduction. Innovative and smart manufacturing methodologies and flows are also becoming increasingly important. Since algorithmic development is changing rapidly, smart manufacturing enabling reduced NRE and faster time to market is critical.

In this annual gathering of electronic IC/system designers and developers, we will discuss design methodologies, design flows and CAD tool needs via presentations or panel discussions. This year, EDPS focuses on areas covering: Cyber Systems Design with emphasis on security, Machine Learning in System Design and EDA, Smart Manufacturing – Increased cooperation between design and manufacturing, Advanced Packaging, IoT, Machine Learning, Cloud manufacturing, Supply Chain Safety, Innovative Designs and Design Techniques, and System reliability with special focus on ADAS and 5G. Please contact Shishpal Rawat (ssrawat@iitkalumni.org) to submit abstract and discuss areas of mutual interest. Complete presentations from 2017 EDPS and previous years are available here.

New DATC Robust Design Flow Database

In recent years, EDA research contests and their released benchmark suites have successfully stimulated research on timely and practical problems and advanced cutting edge technologies. These contests, however, focused on only point tool problems. Robust Design Flow (RDF) Database is developed to direct research attentions to the overall design flow and cross-stage optimizations.

DATC RDF improves the first version published in 2016 to better fit industrial practice. The new DATC RDF includes public academic binaries for logic synthesis, placement, timing analysis, gate sizing, and global routing, as well as additional translation scripts for data exchange between tools. RDF supports standard industrial design input/output formats from the RTL description of circuits all the way to timing constraints. Currently, the RDF database contains: 26 benchmark circuits from the 2017 TAU Timing Contest, 14 logic synthesis scenarios of ABC, 6 placers, 3 routers, 2 gate sizers, and 2 timers.

Users can customize their own flow based on the above options. The RDF includes a cloud version providing detailed runtime information for a customized flow configured by users. In addition, users can download the results from cloud, such as gate-mapped Verilog netlist, placement results in DEF format, global routing results, and timing analysis results.

DATC RDF database is constructed purely based on existing EDA contest results. Future versions will move towards industrial standard OA interface and expand this flow both vertically and horizontally.

Papers in IEEE Design & Test Magazine

The top-five accessed articles from *Design & Test Magazine* in March 2018 were as follows:

- "Approximate Computing: A Survey," by Q. Xu, T. Mytkowicz, and N. S. Kim
- "Security and Privacy in Cyber-Physical Systems: A Survey of Surveys," by J. Giraldo *et al*
- "Time-Critical Systems Design: A Survey," T. Mitra, J. Teich, and L. Thiele
- "Challenges and Trends in Modern SoC Design Verification," by W. Chen *et al*
- "Post-Silicon Validation in the SoC Era: A Tutorial Introduction," by P. Mishra, R. Morad, A. Ziv, and S. Ray

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