September 2013

Currents

2013 CEDA Early Career Award Recipients

CEDA will present two achievement awards during the opening session of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) on 18 November 2013 at the Hilton Hotel in San Jose, California. David Atienza and Zhuo Li will receive this year's Early Career Award for their work in electronic design automation (EDA).

CEDA's Early Career Award honors individuals who have made innovative and substantial technical contributions to EDA in the early stages of their careers. Contributions are evaluated according to the individual's technical merit and creativity in performing research, with consideration of his or her published record and the references accompanying the nomination. The award is equally available to contributors from academic and industrial institutions.

David Atienza is being recognized for his sustained and outstanding contributions to design methods and tools for multiprocessor SoCs (MPSoCs), especially his work on thermal-aware design, low-power architectures, and on-chip interconnects synthesis. Zhuo Li is being recognized for his essential and outstanding contributions to algorithms, methodologies, and software for interconnect optimization, physical synthesis, parasitic extraction, testing, and simulation.

"Professor Atienza and Dr. Li have made important contributions to EDA, and CEDA is pleased to be able to recognize both of them," noted David Yeh, Chair of CEDA's Awards Committee.

David Atienza is an assistant professor of electrical engineering and director of ESL at EPFL, Switzerland. He is also an adjunct professor in the Computer Architecture and Automation Department at Universidad Complutense Madrid (UCM). His research focuses on system-level design methodologies for low-power embedded systems and high-performance SoCs, including new thermal-aware design and management for 2D and 3D MPSoC computing systems; design methods; and architectures for wireless body sensor networks, dynamic memory management, and interconnection hierarchy optimizations. He has an MSc from UCM and a PhD from IMEC, both in computer science and engineering. He is an associate editor of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), *IEEE Design & Test*, and *Elsevier Integration: The VLSI Journal*, and he is a member of CEDA's Executive Committee.

Zhuo Li is a research staff member at IBM Austin Research Laboratory, and he was one of the co-founders of Pextra (a startup specializing in parasitic extraction, later acquired by Mentor Graphics). His research interests include physical synthesis, parasitic extraction, circuit modeling and simulation, and design and analysis of general large-scale algorithms. He has a BS and MS in electrical engineering from Xi'an Jiaotong University, Xi'an, China, and a PhD in computer engineering from Texas A&M University, College Station. He was the Local Program Committee Chair for the 50th Design Automation Conference (DAC). He is currently serving as the secretary of the IEEE Central Texas Section, for which he is the founding chair of the IEEE CEDA Chapter. He is a senior member of IEEE.

For more information, go to http://www.ieee-ceda.org.

New Editorial Team at TCAD in 2014

CEDA is pleased to announce that, starting in January 2014, the next editor-in-chief of *IEEE Transactions on Computer-Aided Design* will be Vijaykrishnan Narayanan (Penn State University). Narayanan is an expert in power-aware and reliable systems, embedded systems, reconfigurable architectures, nano-architectures, and computer architecture. He has published more than 350 papers, with an h-index of 55; has received multiple awards for his research; and is a Fellow of IEEE.

In addition, Charles J. Alpert (IBM Austin Research Laboratory) will serve as deputy editor-in-chief. Alpert has published extensively in the area of physical design. He holds nearly 60 patents and has received three DAC Best Paper Awards. He is the current Technical Program Co-chair for DAC, and he chairs the Design Automation Technical Committee (DATC). He is a Fellow of IEEE.

Interested in volunteering for TCAD? The incoming leadership team will work on formulating the new editorial board over the next few months. If you'd like to serve as an associate editor, please send your CV to Vijaykrishnan Narayanan at vijay@cse.psu.edu before 1 October 2013.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

TCAD *Call for Papers: Special Section on Optical Interconnects*

Increasing interconnect delays over devices at advanced nodes indicate a need for drastic interconnect changes. Such drastic changes are usually possible with material modifications; however, an orthogonal change may be needed soon. In particular, on-chip optical interconnections may be necessary to cope with system-scale performance roadmaps. On-chip optical-interconnect prototypes using standard silicon-based semiconductor processing have already been shown to be possible. However, modeling, design, analysis, prediction, optimization, and CAD tool aspects require practical solutions.

In light of these developments and needs, *IEEE Transactions on Computer-Aided Design* will publish a Special Section on Optical Interconnects, currently planned for April 2014. Original work on optical interconnects should be submitted by 9 September 2013. (Please note that this special section is under a tight schedule, so this deadline is firm.) The following topics are of particular interest:

- Optical interconnect prediction and optimization at various IC design stages
- Optical interconnect design challenges and system-level design for FPGAs and NoCs.
- Reliability prediction of optical interconnects and circuit optimization to mitigate reliability concerns
- Topologies and fabrics of optical interconnects for multi- and many-core architectures
- Design for manufacturability and yield techniques for optical interconnects
- High-speed chip-to-chip optical interconnect design
- Power consumption of optical interconnects
- Co-integration of optical interconnects with 3D chip stacking
- Co-optimization of optical interconnects with chip and/or package design

The complete schedule is as follows:

- **Submission deadline:** 9 September 2013
- **End of first round of reviews:** 9 November 2013
- **Final decisions:** 1 March 2014

The review process will be similar to the usual *TCAD* review, and the quality of accepted papers should be similar to those that are published in regular *TCAD* issues.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in June 2013 were as follows:

- "Reconfigurable Computing in Next-Generation Automotive Networks," by S. Shreejith, S.A. Fahmy, and M. Lukasiewycz
- "Hardware-Assisted Detection of Malicious Software in Embedded Systems," by M. Rahmatian et al.
- "Expanding Gate Level Information Flow Tracking for Multilevel Security," by Wei Hu et al.
- "Formal Methods for Early Analysis of Functional Reliability in Component-Based Embedded Applications," by A. Hazra et al.
- "Wireless Sensor Networks for Pilgrims Tracking," by M. Mohandes et al.

Upcoming Conferences
(David Atienza, david.atienza@epfl.ch)

FMCAD	Portland, Oregon, 20-23 Oct. 2013
ICCAD	San Jose, California, 18-21 Nov. 2013
ASP-DAC	Singapore, 20-13 January 2014

Find us online at www.c-eda.org

IEEE Embedded Systems Letters *is open for submissions. Visit mc.manuscriptcentral.com/les-ieee*

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).