SMACD 2017 EDA Competition

The 2017 edition of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2017) was held in Giardini Naxos-Taormina, Italy, from 12th to 15th June 2017, with the technical sponsorships of IEEE, IEEE Circuits and Systems Society (CASS) and IEEE Council on Electronic Design Automation (CEDA).

Since several editions, SMACD organizes an EDA students' Competition, where MSc and PhD students can compete with their best ideas, methodologies, flows, and tools with one unique but challenging goal: "*Improving design automation for integrated circuits and systems*". Every year the number of papers and live demos proposed for the Competition is increasing, as well as the quality and the potentiality of the proposed solutions. A $1,000 prize has been granted to the winner of the Competition. IEEE CEDA has also promoted the event, funding 500$ of the total prize.

The 2017 edition of the Competition has been co-organized by Rafael Castro-Lopez (CSIC and University of Seville, Spain) and Ralf Sommer (Ilmenau University of Technology, Germany). In two dedicated sessions of the conference, the best six proposals and ideas were presented by the students. A committee of experts from academia and industry interacted with the students during the sessions and selected the winner of the Competition based on the quality of the paper, its presentation, and its live demo. The Competition prize was granted to Axel Hald, from Automotive Electronics Robert Bosch GmbH, Germany. His paper entitled "*A New Method for the Analysis of Movement Dependent Parasitics in Full Custom Designed MEMS Sensor*" (Co-Authors: J. Seelhorst, P. Herzogenrath, J. Scheible and J. Lienig) was awarded during the SMACD 2017 gala dinner.

More details on the Competition are available at http://smacd2017.unisa.it/?id=callcomp

Recipient of the Accellera Systems Initiative 2017 Leadership Award

Congratulations to Shishpal Rawat, President of CEDA, as the recipient of the Accellera Systems Initiative 2017 Leadership Award. The award recognizes the vision, leadership, and contribution to standards development, governance and promotional activities of an Accellera member on behalf of the organization. The award was presented to Shishpal at the 54th Design Automation Conference (DAC) during the Accellera Breakfast and Portable Stimulus Town Hall on Tuesday, June 20.

"Shishpal has had a profound impact on the advancement of Accellera's mission and its growth worldwide," stated Lu Dai, Accellera Systems Initiative Chair. "We are grateful for his years of leadership and dedication. Among his many accomplishments during his tenure as Chair of the Board of Accellera from 2010-2016, 15 members were added worldwide, three standards were published and two of those standards were successfully delivered to the IEEE Standards Association (SystemC AMS and UVM). He is very deserving of this award, and I am proud to honor him among his colleagues at DAC."

"I am deeply honored by this recognition from Accellera," stated Dr. Shishpal Rawat. "With the help of key leaders in Accellera, we were able to expand the technical scope of Accellera and also market its standards across the globe at multiple DVCon conferences. These standards continue to have a positive impact on the productivity of chip design and design tools. I look forward to continued collaboration with Accellera."

Shishpal has more than 30 years of experience in the electronics industry. He held a variety of positions at Intel Corporation prior to his retirement last year, most recently as Director of external EDA strategy.

Shishpal became chair of Accellera in June 2010. As chair of Accellera, he oversaw the consolidation of standards bodies, namely the merger with OSCI, as well as the acquisition of the OCP standard. He also helped to extend the relationship with the IEEE Standards Association's IEEE Get Program for an additional 10 years, ensuring continued public access to view and download current EDA standards at no charge, courtesy of Accellera. He

managed the relicensing of SystemC contributions to Apache 2.0 and oversaw the move toward standardization of the Universal Verification Methodology (UVM) standard to IEEE 1800.2. The Verilog AMS standard also moved under the SystemVerilog AMS standard. The deployment of Accellera standards via the DVCon brand of conferences expanded to Europe and India, and the planning and development for DVCon China were initiated during his term of leadership. Most recently, the emerging Portable Stimulus standard made significant strides since work began in 2015 while Shishpal was chair of Accellera.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in June 2017 were as follows:

- "Testing Autonomous Vehicle Software in the Virtual Prototyping Environment," by B. Kim et al.
- "Energy Efficient Outdoor Light Monitoring and Control Architecture Using Embedded System," by Z. Kaleem, T.M. Yoon, and C. Lee
- "Public Key Authentication and Key Agreement in IoT Devices With Minimal Airtime Consumption," by S. Sciancalepore et al.
- "Arduino Debugger," by J. Dolinay et al.
- "Wearable Camera- and Accelerometer-Based Fall Detection on Portable Devices," by K. Ozcan and S. Velipasalar

Papers in IEEE Design and Test

The top-five accessed articles from *IEEE Design and Test* in June 2017 were as follows:

- "Recent Technology Advances of Emerging Memories," by Y. Chen et al.
- "Security and Privacy in Cyber-Physical Systems: A Survey of Surveys," by J. Giraldo et al.
- "Computing in the Dark Silicon Era: Current Trends and Research Challenges," by M. Shafique et al.
- "Post-Silicon Validation in the SoC Era: A Tutorial Introduction," by P. Mishra et al.
- "Approximate Computing: A Survey," by Qiang Xu et al.

Upcoming Conferences (Yao-Wen Chang, ywchang@ntu.edu.tw)	
FMCAD	TU Wien, Vienna, Austria - October 2-6
ESWEEK	Seoul, Korea - October 15-20
NOCS	Seoul, Korea - October 19-20

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