September 2018

Currents

CEDA

IEEE Council on Electronic Design Automation

Electronic Resurgence Initiative Summit

On July 23-25, DARPA held its Electronic Resurgence Initiative (ERI) Summit at San Francisco's Palace of Fine Arts. The summit, led by Dr. Bill Chappell (Director of DARPA's Microsystems Technology Office), brought together researchers and program managers across academia, industry, and government. In his opening keynote, Dr. John Hennessy (Alphabet, Stanford) emphasized the rise of domain-specific architectures, the role of hardware-software co-optimization, and the importance of engineers (and not just physicists) in the creation of new technologies such as carbon nanotubes or quantum computing. The ERI Summit featured DARPA's research initiatives, including six new programs, across its three "Page 3" thrusts: Materials and integration, Electronic Design Automation (EDA), Architecture and Applications.

Dr. Mike Mayberry (Intel) and Mr. Gary Dickerson (Applied Materials), in their keynotes on materials and integration, highlighted the importance of new materials and 3D integration for the path forward as traditional approaches to semiconductor scaling slow down. Mr. Dickerson announced Applied Materials' collaborative effort in Correlated-Electron RAM.

Dr. Max Shulaker (MIT) and Dr. Subhasish Mitra (Stanford) presented their joint team effort as part of DARPA's new 3DSoC (3D System-on-Chip, under Dr. Linton Salmon) program. MIT and Stanford will jointly create new monolithic 3D architectures with computation immersed in memory, uniquely enabled by carbon nanotube field-effect transistors and Resistive RAM, for drastic energy and execution time benefits especially for abundant-data applications (e.g., machine learning-based AI). They will work together with Skywater Technology Foundry to create the foundational technologies and fabricate such monolithic 3D chips. As part of DARPA's FRANC (Foundations Required for Novel Compute, under Dr. Young-Kai Chen) program, Mr. Steve Pawlowski (Micron) and Dr. Naresh Shanbhag (UIUC) also highlighted the energy and execution time costs of data movement, and outlined their approaches that include ideas such as computation inside memory arrays.

Dr. Aart de Geus (Synopsys) delivered the EDA thrust keynote. Mr. Andreas Oloffson (DARPA program manager) presented the vision for his new DARPA programs IDEA (Intelligent Design of Electronic Assets) and POSH (Posh Open Source Hardware): create a silicon compiler for design specification to complete chip layout within 24 hours, with just a press of a button; and, create a wide variety of open-source hardware IP, ranging from processors to FPGAs to analog circuits, together with quick and automatic verification techniques, pre-silicon and post-silicon.

Among various speakers, Dr. Andrew Kahng (UCSD) presented his team's IDEA project on an automated open-source tool that can perform tapeout-ready layout of an SoC within 24 hours. His project will leverage breakthroughs in partitioning, optimization, and machine learning techniques. Dr. Clark Barrett (Stanford) presented his team's POSH effort on dramatically improving verification by leveraging latest open-source SMT (Satisfiability Modulo Theories) solvers, as well as Symbolic Quick Error Detection to detect large classes of difficult design bugs automatically (without writing properties or assertions) and quickly (minutes for IP blocks, overnight for billion-transistor-scale designs).

Dr. Bill Dally (NVIDIA, Stanford), in his architecture thrust keynote, highlighted the importance of parallelism, as embodied by compute devices such as GPUs, and the use of parallelism-friendly software. Two new architecture programs were announced: DSSoC (Domain-Specific System-on-Chip, under Dr. Tom Rondeau) and SDH (Software-Defined Hardware, under Mr. Wade Shen). Among various speakers, Dr. Luca Carloni (Columbia) presented his team's SDH approach using a coarse-grained reconfigurable fabric which leverages runtime information for memory access efficiency. The ERI applications thrust sessions featured a keynote by Dr. Wally Rhines (Siemens/Mentor Graphics) followed by several speakers covering security, trust, sensors, spectrum collaboration challenge, and lifelong learning-based AI.

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The ERI Summit concluded with a panel where DARPA program managers discussed several future directions, including new approaches to AI, new system synthesis and emulation, photonics, security and trust.

2018 IEEE International Smart Cities Conference

The IEEE 4th Annual International Smart Cities Conference (ISC2 2018) will be held in Kansas City, MO, USA on 16-19 September. As the flagship conference sponsored by the IEEE Smart Cities Initiative, ISC2 2018 brings together researchers and practitioners in a collaborative smart cities discussion, including scholars, citizens, policymakers, administrators, infrastructure operators, industry representatives, economists, sociologists, and academicians. Technical exchanges within the research community will encompass panels, plenary talks, technical sessions, tutorials, workshops and exhibitions.

CEDA is one of the Partner Organizational Units of IEEE Smart Cities and will actively participate in the conference. Prof. Jose Ayala, VP Initiatives of CEDA, will present CEDA's activities and perspectives during a panel session discussing "The Roles of IEEE Smart Cities Technical Community – Perspectives from Contributing Technical Societies," on September 17th.

EDAthon 2018 by Hong Kong Chapter

On July 8, the IEEE CEDA Hong Kong chapter held the ISVLSI-EDAthon 2018 with twelve 2-member teams coming from universities across mainland China, Hong Kong, Taiwan, and Korea. During the one-day competition, all participants exercised their sophisticated coding and analytical skills to solve interesting EDA problems.

EDAthon is a whole-day programming contest that features interesting and challenging topics in Electronic Design Automation (EDA). It is also a unique opportunity to bring together talents for EDA which enables the rapid advancement in computer technology. The contest will involve solving interesting problems in the broad context of Computer-Aided Design (CAD) of integrated circuits and systems, including problems selected from the following areas: System Design and Analysis, Logic and High-level Design, Physical Design, and Circuit Analysis, and Emerging Technologies. The contest emphasized team work, problem solving skills and programming techniques for EDA applications. It is a goal of EDAthon and CEDA Hong Kong Chapter to promote EDA in Hong Kong and her neighboring regions, and to nurture the best of the next-generation students and professionals for the EDA community.

The three awarded teams for their outstanding performance were: Feng Wang and Zhuolun He from Peking University (Champion), Huang Zhaoyuan and Li Wangyang, from the National Tsing Hua University (2nd place), and Jia-Shiuan Chen and Shih-Yu Chuang, from the National Taiwan University (3rd place).

IoT Summer School

On August 6-10, the first IoT summer School was held by Prof. Marilyn Wolf of Georgia Tech on its Atlanta Campus. In addition to CEDA's support, the event was sponsored by ARM and received additional support from VMware. The summer school hosted 40 graduate students and academics from across U.S and Europe. Other attendees included industry professionals from VMware.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in July 2018 were as follows:

- "A Taxonomy of General Purpose Approximate Computing Techniques," by T. Moreau *et al.,*
- "Multipliers With Approximate 4–2 Compressors and Error Recovery Modules," by M. Ha and S. Lee
- "A Novel Heterogeneous Approximate Multiplier for Low Power and High Performance," by I. Alouani, H. Ahangari, O. Ozturk, and S. Niar
- "Tactics to Directly Map CNN Graphs on Embedded FPGAs," by K. Abdelouahab, M. Pelcat, J. Sérot, C. Bourrasset, and F. Berry
- "Testing Autonomous Vehicle Software in the Virtual Prototyping Environment," by B. Kim, Y. Kashiba, S. Dai, and S. Shiraishi

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