April 2012 CEDA Currents

IEEE Council on Electronic Design Automation

IEEE Design and Test *Call for Papers: Special Issue on Practical Parallel EDA*

Future advances in computing performance will not be driven by increases in individual core performance, but rather by factors such as an increasing number of available processors or specialized hardware. Successful EDA engineers and software developers must become familiar with parallel algorithms and methods to exploit parallel and specialized computing resources.

Sequential EDA algorithms of the past are not keeping pace with increasing design complexity. Hence, there is a striking need to apply parallel-computing methods to EDA problems. Execution of software on parallel-computing platforms requires reengineering the EDA tools used during VLSI design. Although there are experts in various domains of parallelism, the knowledge has yet to be dispersed widely and used in a variety of EDA tools. Attaining knowledge in parallelism requires understanding it from many aspects.

For example, not only are parallel algorithms typically different than serial ones but the programming methods and tools are also often significantly different. The availability of low-cost parallel-processing hardware has made this transformation both possible and increasingly relevant.

IEEE Design and Test seeks contributions for a special issue to educate engineers and present recent work in the area of practical parallelism in EDA. Algorithm implementation can target various parallel architectures, such as GPUs, multicore CPUs, many-core CPUs, distributed systems, advanced processing units, and FPGAs. *D&T* also encourages submission of papers that point to practical limitations of parallelism in EDA.

Topics of interest include, but are not limited to

- parallel algorithms for EDA;
- performance comparison of parallel-programming methods for EDA algorithms;
- performance comparison of parallel architectures for a given EDA algorithm or set of algorithms;
- performance comparison of EDA algorithms or sets of algorithms implemented on various parallel architectures;
- tips and tricks of a parallel implementation from a real product;
- user perspectives from parallel-EDA software users;
- practical limitations of parallel-EDA algorithm implementations; and
- cost and benefit analysis of parallel EDA.

Submission and Review Process

Prospective authors should follow the submission guidelines for *IEEE Design & Test*. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/cs-ieee. Indicate that you are submitting your article to the special issue on Practical Parallel EDA. All articles will undergo the standard *IEEE Design & Test* review process. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere.

Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 References (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see *IEEE Design & Test* Author Resources at http://www.computer.org/dt/author.htm, then scroll down and click on Author Center for submission guidelines and requirements.

Schedule

- Manuscripts due: 15 April 2012
- Reviews completed: 15 June 2012
- Revisions due: 15 July 2012
- Final version due: 1 September 2012
- Publication: Jan./Feb. 2013

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

Embedded Systems Week Call for Papers

Embedded Systems Week will take place in Tampere, Finland, on 7-12 October 2012. This year, ESWeek will be colocated with the International Symposium on System-on-Chip (SoC 2012).

ESWeek is a premier event covering all aspects of embedded systems and software. It brings together conferences, tutorials, and workshops centered on various aspects of embedded systems research and development.

Three leading conferences will take place during ESWeek: the International Conference on Compilers Architecture and Synthesis for Embedded Systems (CASES 2012), the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2012), and the International Conference on Embedded Software (EMSOFT 2012). This will allow attendees to benefit from a wide range of topics covered by these conferences and their associated tutorials and workshops.

The paper submissions schedule is as follows:

- Abstracts due: 28 March 2012
- Full paper submission: 4 April 2012
- Acceptance notification: 3 July 2012
- Camera-ready version: 31 July 2012

For details and instructions regarding paper submissions, see http://www.esweek.org.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in December 2011 were as follows:

- "Data Archival to SD Card via Hardware Description Language," by O. Elkeelany et al.
- "PI and PID Regulation Approaches for Performance-Constrained Adaptive Multiprocessor System-on-Chip," by G.M. Almeida et al.
- "Opal: A Multiradio Platform for High Throughput Wireless Sensor Networks," by R. Jurdak et al.
- "Efficient On-Chip Task Scheduler and Allocator for Reconfigurable Operating Systems," by C.H. Benkrid et al.
- "A Novel Soft Error Detection and Correction Circuit for Embedded Reconfigurable Systems," by Q.Z. Ichinomiya et al.

Upcoming Conferences (David Atienza, david.atienza@epfl.ch)	
GLSVLSI	Salt Lake City, 3-4 May 2012
NOCS	Lyngby, Denmark, 9-11 May 2012
DAC	San Francisco, 3-7 June 2012
VLSI-SoC	Santa Cruz, Calif., 7-10 October 2012

IEEE Embedded Systems Letters *is open for submissions. Visit mc.manuscriptcentral.com/les-ieee*

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