January 2013

Currents

IEEE Council on Electronic Design Automation

VLSI-SoC 2012 Report

The IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) explores the state of the art and the latest developments in very large-scale integration (VLSI) and SoCs. The 20th annual VLSI-SoC was held on 7 to 12 October 2012 in Santa Cruz, California.

VLSI-SoC 2013 received 119 submissions. These included 106 regular scientific papers, from which the 115 members of the technical program committee selected 33 papers for oral presentation and 17 posters. Oral presentations and posters are presented in the proceedings with six-page regular papers and four-page short papers, respectively. The conference continues to follow its track record of being highly selective to ensure a high-quality technical program with a full-paper acceptance rate of 31%.

In addition to the regular paper and poster sessions, there were two special sessions this year devoted to the emerging topic of memristive computing, and to open-source tools and methodologies for research.

The program also included three outstanding keynotes: "Design and Testing Strategies for Modular 3D-Multiprocessor Systems," by Yusuf Leblebici (EPFL); "A Roadmap for DFM and Physical Design at the Limits of IC Scaling," by Luigi Capodieci (GlobalFoundries); and "High Performance Ray Tracing: Implications for System Architectures," by Erik Brunvand (University of Utah).

A panel session was held on "Analog VLSI Design at the End of CMOS Scaling: What Is Ahead?" There was also an embedded tutorial on "Silicon Photonics Circuits and Architectures for Many-Core Systems." Finally, the program included a successful PhD Forum with 17 posters.

The best paper award for the conference was given to Neil Di Spigna, Daniel Schinke, Srikant Jayanti, Veena Misra, and Paul Franzon (North Carolina State University) for their paper "A Novel Double Floating-Gate Unified Memory Device."

The proceedings of the conference are published by IEEE, and extended versions of the papers will be published in a post-conference book by Springer under an agreement with the International Federation for Information Processing (IFIP).

The next VLSI-SoC conference will take place in Istanbul, Turkey, on 7 to 9 October 2013. The call for papers is available at http://www.vlsisoc2013.ozyegin.edu.tr.

Ayse Coskun and Andreas Burg (Technical Program Co-chairs); Matthew Guthaus (General Chair)

ICCAD 2012 Awards

The **ICCAD Ten Year Retrospective Most Influential Paper Award** is given to the paper judged to be the most influential on research and industry practice in CAD of ICs over the 10 years since its original appearance at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD). This year's winner was the 2002 paper "Combined Dynamic Voltage Scaling and Adaptive Body Biasing for Lower Power Microprocessors under Dynamic Workloads," by Steven M. Martin, Krisztian Flautner, Trevor Mudge, and David Blaauw.

The **IEEE/ACM William J. McCalla ICCAD Best Paper Award** is given in memory of William J. McCalla for his contribution to ICCAD and his CAD technical work throughout his career. This year's winner was the paper "Stability Assurance and Design Optimization of Large Power Delivery Networks with Multiple On-Chip Voltage Regulators" by Suming Lai, Boyuan Yan, and Peng Li.

Upcoming CEDA Award Nominations

Nominations are being accepted for the following awards, with the deadlines indicated in the table below.

Award Name	**Nomination Deadline**
Phil Kaufman Award	31 January 2013
A. Richard Newton Technical Impact Award	1 February 2013
IEEE CEDA Distinguished Service Award	15 March 2013
IEEE CEDA Early Career Award	15 April 2013

For more information, please visit www.c-eda.org.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

Phil Kaufman Award Ceremony at 50th Design Automation Conference

The 2013 Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation ceremony will be held on 2 June 2013 at the 50th Design Automation Conference (DAC) in Austin, Texas. The sponsors of this award are the CEDA (www.c-eda.org) and the EDA Consortium (EDAC) (www.edac.org).

"This is an opportunity for the entire EDA and DAC community to honor the Phil Kaufman Award recipient," said Donatella Sciuto, president of CEDA. "It's also a way to celebrate 50 years of the Design Automation Conference by highlighting an individual's significant achievements."

Since the Phil Kaufman Award ceremony will now be held at DAC, the call for nominations has been extended until 31 January 2013. All current and past nominations will be considered. Nomination forms are available at http://www.edac.org/about_kaufman_award.jsp#nominations.

For more information, go to: www.c-eda.org.

Call for Papers for ACM Transactions on Design Automation of Electronic Systems

ACM Transactions on Design Automation of Electronics Systems is planning a special section on Networks on Chip: Architecture, Tools, and Methodology. This special section will report on recent advances in the development of on-chip communication technology, architecture, design methods, and applications, while encouraging innovation from interrelated research communities, including computer architecture, networking, circuits and systems, embedded systems, and design automation. Topics include network architecture (topology, routing, arbitration); network design for 3D stacked logic and memory; mapping of applications onto NoCs; power and energy issues; timing; synchronous/asynchronous communication; and NoC reliability issues.

Authors are encouraged to submit high-quality research contributions that will not require major revisions. Extensions of papers presented at the 6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2012) (http://www.nocsymposium.org) are especially encouraged. Please clearly identify the additional material from the original symposium paper in your submitted manuscript. Submissions of relevant original work not presented at NOCS 2012 are also welcome. All manuscripts are subject to the standard ACM review process. Please submit your manuscripts electronically at http://mc.manuscriptcentral.com/todaes, where instructions on how to submit papers can also be found.

Important dates are as follows:

- **Manuscript Due:** 18 January 2013
- **Notification Date:** 26 April 2013
- **Final Version Due:** 7 June 2013

Please identify your papers as submissions for the "Special Section on NOC: ATM 2012," both on your manuscript and in the Web submission form's Note to Editor field.

Contact Annie Yu (todaes@ceng.usc.edu) for further assistance.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in September 2012 were as follows:

- "Design and Implementation of a Virtual Platform of Solid-State Disks," by Y.-C. Lee, C.-T. Kuo, and L.-P. Chang
- "Hardware-Assisted Detection of Malicious Software in Embedded Systems," by M. Rahmatian et al.
- "Block-Based Major Color Method for Foreground Object Detection on Embedded SoC Platforms," by W.-K. Tsai, M.-H. Sheu, and C.-C. Lin
- "Comparison of Preemption Schemes for Partially Reconfigurable FPGAs," by K. Jozwik et al.
- "Power Variability in Contemporary DRAMs," by M. Gottscho, A.A. Kagalwalla, and P. Gupta

Upcoming Conferences (David Atienza, david.atienza@epfl.ch)	
ASP-DAC	Yokohama, Japan, 22-25 January 2013
DATE	Grenoble, France, 18-22 March 2013
GLSVLSI	Paris, France, 2-4 May 2013
NOCS	Tempe, Arizona, 21-24 April 2013
DAC	Austin, Texas, 2-6 June 2013

IEEE Embedded Systems Letters ***is open for submissions. Visit mc.manuscriptcentral.com/les-ieee.***

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).