August 2011 Currents

CEDA

IEEE Council on Electronic Design Automation

CEDA Awards

The following individuals have been honored with awards from IEEE CEDA.

Jason Cong (University of California, Los Angeles) and Yuzheng Ding (Xilinx) have won the ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation for their article, "FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs." This article was published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 1, Jan. 1994, pp. 1-12.

The ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation rewards pioneering work in technology mapping for FPGAs that significantly impacts the FPGA research community and industry.

Sachin Sapatnekar (University of Minnesota, Minneapolis) has been honored with the IEEE CEDA Outstanding Service Contribution award for his outstanding service as General Chair of the 2010 Design Automation Conference (DAC). This award honors outstanding service that benefits IEEE CEDA.

Finally, Amith Singhee (IBM T.J. Watson Research Center) and Rob A. Rutenbar (Carnegie Mellon University) have won the IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award for their article, "Statistical Blockade: Very Fast Statistical Simulation and Modeling of Rare Circuit Events and Its Application to Memory Design." This article was published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 8, Aug. 2009, pp. 1176-1189.

EDP 2011 – A Breath of Fresh Air

It's really nice to sit in a presentation about cloud computing that isn't a marketing pitch—a presentation from engineers, for engineers, that considers the pros and cons of the technology and puts the market in its proper perspective.

The 2011 Electronic Design Processes Symposium (EDP) had three of them. It's also nice to have an entire session on 3D ICs that takes the same approach. That's why I come back to EDP every year.

Parallel-Programming Breakthroughs

This year's talks on parallel computing focused on EDA tools. In 2009, we hit a wall; we had done what we could before running into Amdahl's law. In 2010, we started working on the hard stuff. In 2011, we are seeing results. Now that we have a better understanding of the problem, we can more easily modify existing code to run on parallel machines.

Most interesting are the breakthroughs we're seeing in parallel algorithmic development. This is what Gene Amdahl was talking about when he said we would have to rewrite the algorithms.

Once application developers fully understand the problem, we can expect major advances in their parallel algorithms. EDA is already at that point—perhaps the first application area to get there. This is what we do, this is what we have always done: develop state-of-the-art algorithms.

An Honest Look at Cloud Computing

James Colgan (Xuropa) gave a good talk on how the cloud can be used by EDA vendors. Colgan promoted both a marketing use of the cloud and adoption by the long tail of EDA users.

Naresh Sehgal and Ed Grochowski of Intel talked about using an internal cloud for design. Grochowski's talk favored the typical semiconductor client-server approach, in which the big computing jobs are sent out to the cloud, while most of the work still occurs on the engineer's desktop. Latency is a big problem using only the cloud.

One thing that dawned on me while watching the presentations is that cloud promoters all assume we will continue using symmetric multiprocessing (SMP), or homogeneous multiprocessing—the PC model of computing.

Increasingly, however, more technologists are looking at asymmetric multiprocessing (AMP), or heterogeneous multiprocessing—a commonly used computing model on cell phones. If the latter becomes the norm, it will favor the in-house or EDA vendor's cloud model rather than the generic Amazon-type cloud.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es) or Rajesh Gupta.

3D IC Is Progressing

Although there's still some talk of seven-high stacks of logic chips or ten-high stacks of logic, analog, RF, and memory chips, the reality is that 2.5D is the norm, with memory stacked on logic and with analog and RF chips separate on an interposer. We're still waiting for through-silicon vias (TSVs) to be practical, and this is expected to happen around 2014 or 2015.

My feeling is that 3D IC will take over the job of Moore's law from plain old CMOS sometime in the next decade, but it will just be a gap filler until spintronics, or something else, takes over.

Gary Smith, GSEDA (www.garysmitheda.com)

Nano-Tera Holds Its 2nd Annual Meeting

The 2nd Annual Plenary Meeting of Nano-Tera was held in Bern, Switzerland, on 12-13 May 2011. Nano-Tera supports research in the engineering of complex systems for health, security, and the environment using micro- and nanotechnologies, considering key energy aspects.

This year's program centered on the mission of bringing Switzerland to the forefront of a new technological revolution. The convergence of technologies in these areas represents fertile ground for innovation; this convergence will be instrumental in the development of new markets and improvement in quality of life.

The meeting featured a keynote presentation by Bruno Murari (STMicroelectronics) entitled, "Lateral Thinking: The Impact on Breakthrough Innovation." There were also oral presentations by all principal investigators to the 19 large-scale projects. In addition, 107 posters were presented by researchers involved in various fields, from health and environmental-monitoring devices to sensing techniques, computing, and communications.

Nano-Tera has recently attracted additional industrial contributions toward preselected projects such as Nokia (OpenSense), IBM (NexRay), STMicroelectronics (ISyPeM), and smaller players. This community of leading experts addresses interdisciplinary and interinstitutional projects, and the competitive convergence resulting from it is building strength toward providing further deployment.

For example, a recently launched call for proposal (CFP) for a joint pilot grant between Nano-Tera and the Sino-Swiss Science and Technology Cooperation (SSSTC) aims at creating synergies to encourage Swiss-Chinese research collaborations within Nano-Tera thematic areas, anticipating the importance of setting norms as a driver for innovation. This funding fits into the context of the recent strengthening of ties between China and Switzerland, reinforcing common programs in sectors such as health, the environment, and energy.

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Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in March 2011 were as follows:

- "Control Focused Soft Error Detection for Embedded Applications," by K. Shankar and R. Lysecky
- "Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles," by C. Spelta et al.
- "Fault Classification for SRAM-Based FPGAs in the Space Environment for Fault Mitigation," by C. Bolchini and C. Sandionigi
- "Minimum-Energy Operation via Error Resiliency," by R.A. Abdallah and N.R. Shanbhag
- "Reconfigurable Architecture for ZQDCT Using Computational Complexity Prediction and Bitstream Relocation," by J. Huang and J. Lee

Upcoming Conferences (Bill Joyner, william.joyner@src.org)	
PATMOS	Madrid, 26-29 September 2011
VLSI- SoC	Hong Kong, 3-5 October 2011
FMCAD	Austin, Texas, 30 Oct.-2 Nov. 2011
ICCAD	San Jose, Calif., 6-10 November 2011

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