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CEDA Currents

IEEE Council on Electronic Design Automation

Adressing Thermal Issues in 3D Stacks in the Nano-Tera CMOSAIC Project

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Continuous technical advances are fueling the trend toward more sophisticated and high-performance chip designs, increasing functionality and clock rates while shrinking the feature sizes. Interconnects have not followed the same scaling curve as transistors, hence they have become a limiting factor in performance and power consumption.

One solution to the problem of the rising power consumption in interconnects is 3D stacking, which reduces the length of the communication lines through vertical integration of circuit blocks. However, 3D stacking substantially increases power density due to the placement of computational units on top of each other. High power densities are already a major concern in 2D circuits, and in 3D systems the problem is even more severe. The 3D stacked systems exacerbate temperature-induced problems, leading to degraded performance and reliability if not handled properly.

The CMOSAIC project is a genuine opportunity to contribute to the realization of arguably the most complicated system that mankind has ever assembled: a 3D stack of computer chips with a functionality per unit volume that nearly parallels the functional density of a human brain. CMOSAIC's aggressive goal is to provide the necessarily 3D integrated cooling system that is the key to compressing almost 1012 nanometer sized functional units (1 Tera) into one cubic centimeter with a 10 to 100 fold higher connectivity than otherwise possible. Even the most advanced air-cooling methods are inadequate for high performance 3D-IC systems where the main challenge is to remove the heat produced by multiple stacked dies in a 1-3 cm3 volume, each layer dissipating 100-150 W/cm2. State-of-the-art single phase liquid and two- phase cooling systems, using specifically designed microchannel arrangements, and employing coolants ranging from liquid water and two-phase environmentally friendly refrigerants to novel engineered nanofluids offer significant advantages in addressing heat removal challenges leading to practical 3D systems. CMOSAIC aims at developing the engineering science base that will enable a new state of the art in high density electronics cooling.

Specifically, this project brings together internationally recognized experts of leading Swiss universities and industry (EPFL, ETH Zurich and IBM Research Laboratory in Rüschlikon) to thoroughly investigate this interdisciplinary problem at different levels (architecture, microfabrication, liquid cooling, two-phase cooling, nanofluids). These experts are joining forces to research the related physics and to develop the necessary thermal/electronic computational tools/methods. The project includes an intensive experimental program, consisting of challenging flow visualizations and heat transfer measurements in microchannel systems of hydraulic diameter often comparable to or smaller than that of a human hair, with complex fluids flowing through them. It also targets the development of novel theoretical models explaining the physics and new electronics packing models together with new micro- manufacturing processes. The verification of the proposed novel approaches coming out of this project will be conducted using several prototypes that will be built and tested. With respect to the Nano-Tera.CH proposal, this project addresses the vertical axis of micro/nanoelectronics, particularly the aspect of system integration. Specifically, the results of this project will be a significant step toward "achieving system complexities that are two-to- three orders of magnitude higher than today's state-of-the-art", by developing the fundamental understanding, methods and tools required for efficient and reliable design of true 3D integrated circuit systems.

CMOSAIC is one of the most ambitious projects in the field of 3D chips, covering many different areas of research and targeting the goal at different abstraction levels. Only the joint work of research experts and industrial partners allows the persecution of such interesting objectives. Please visit the following website for further information: http://www.nano-tera.ch/projects/67.php

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CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala, jayala@fdi.ucm.es or Rajesh Gupta.

IEEE Navigation Tool

IEEE is developing a new technology discovery and navigation system to enable professionals and researchers to find conferences, publications and other resources that match their technical interests. In this regard, IEEE has identified 14 market sectors and CEDA will join this initiative by providing tags for each sector in EDA, which will be stored in a global IEEE database. Also, there will be an automated process for mapping EDA-related conferences and publications to the different identified sectors.

The final objective of this initiative is to provide an interface for professionals that help them in finding connections between industry, research and IEEE products and services. This new tool is complementary to other services already provided by IEEE, such as Xplore, or external services from other entities, such as Google Search. The plan is to make this new IEEE Navigation Tool available to the public at the end of the first quarter of 2009, and CEDA is working on making this new tool accessible to EDA professionals directly from its website.

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IEEE's 125 Anniversay

In 2009, IEEE commemorates 125 years of fostering technological innovation and excellence for the public good. Although 13 May 2009 is IEEE's official Anniversary date, the "Engineering the Future" celebration will include a year full of activities, events and the first IEEE Presidents' Change the World Competition for students. And, what is even more appealing, everyone can be a part of IEEE's Anniversary Celebration.

The schedule of the planned activities for this year of celebrations is growing up everyday with new proposals. Among others, these are some of the 125th Anniversary activities: the IEEE Presidents' Change the World Competition (where the winning submission will receive US $10,000 in June 2009 at the Annual IEEE Honors Ceremony), the IEEE125.org (website that centralizes all the information about the 125th Anniversary activities), IEEE Engineering the Future Media Roundtable (media event scheduled for March 10 in New York), IEEE Global Engineering the Future Day (on 13 May 2009, IEEE's official anniversary) and the IEEE Global Engineering the Future Series (eight events planned all around the world: Austin, Bangalore, Tokyo, Beijing, Boston, London, Munich and San Jose).

For further information, please visit http://www.ieee125.org

IFIP Working Group 10.5. Design and Engineering of Electronic Systems

IFIP is the leading multinational, apolitical organization in Information & Communications Technologies and Sciences, recognized by United Nations and other world bodies. It represents IT Societies from 56 countries or regions, covering all 5 continents with a total membership of over half a million; and it links more than 3500 scientists from Academia and Industry, organized in more than 101 Working Groups reporting to 13 Technical Committees. The Working Group 10.5 "Design and Engineering of Electronic Systems" belongs to the IFIP Technical Committee 10. It was established in 1994 by merging the old 10.2 and 10.5 working groups.

The Working Group aims at providing a forum amongst creative experts to explore problem areas and solutions for the design of complex electronic systems and also disseminating the solutions to a broader industrial and educational sphere. The Working Group targets a broad range of topics related to the design and engineering of heterogeneous systems, containing hardware, software, and even mechanical parts. In summary, its main areas of interest are, among others: System Design Methods, Embedded Systems, Modeling and Specification, Design Validation, Reconfigurable Computing, VLSI Systems and Applications, Power-aware Design, Analog and Mixed-Signal Systems, Fundamental CAD Algorithms, etc.

The next meeting of the IFIP WG 10.5 will take place in Nice during the DATE 2009 conference and will provide and excellent environment for the technical discussions of the IFIP members.

For more information, please visit the website of the WG: http://www.inf.ufrgs.br/ifip10-5/index.html

Upcoming Conferences/ Bill Joyner, william.joyner@src.org	
DATE	Nice (France), April 20-24, 2009
GLSVLSI	Massachusetts (USA), May 10-12, 2009
NOCS	San Diego (USA), May 10-13, 2009
MEMOCODE	Cambridge (USA), July 13-15, 2009
DAC	San Francisco (USA), July 26-31, 2009
MPSOC	Georgia (USA), August 2-7, 2009
PATMOS	Delft (Netherlands), Sept. 9-11. 2009
CODES+ISSS	Grenoble (France), Oct. 11-16, 2009
ICCAD	San Jose (USA), November 2-5, 2009
NANO-NET	Switzerland, October 18-20, 2009
FMCAD	Austin (USA), November 2009

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