MARCH 2006

Currents

Council on Electronic Design Automation

CEDA Distinguished Speaker Series

Contributed by Andreas Kuehlmann and Chuck Shaw, {kuehl, shaw}@cadence.com

The *Council*'s Distinguished Speaker Series will feature in-depth presentations of the best works in EDA over the past year, as demonstrated by their reception at our top conferences - such as International Conference on Computer Aided Design (ICCAD) and the Design Automation Conference (DAC) - and IEEE Transactions on Computer Aided Design. Each presentation, which will take place before an audience of experts, will be followed by discussion. Videos of the events will be posted on the *Council*'s Web site.

"The Distinguished Speaker Series is the first of many value-added programs that CEDA will offer IEEE members with an interest in design automation," says **Andreas Kuehlmann**, the *Council*'s vice president of Technical Activities. "We believe it will give designers, researchers, and others a more comprehensive look at the latest breakthrough technologies and developments in this vital, thriving, and exciting community."

Winner of the 2005 IEEE/ACM William J. McCalla ICCAD Best Paper Award, **Zhenhai Zhu** of Cadence Berkeley Labs will kick off the series. Zhu will present *FastSies: A Fast Stochastic Integral Equation Solver for Modeling the Rough Surface Effects* during the Silicon Valley Chapter of the IEEE Solid State Circuits Society meeting on **15 May** at 7 p.m. The meeting will be held at Cadence Design Systems' San Jose headquarters at 2655 Seely Ave., Bldg. 5.

Update from IEEE Transactions on Computer Aided Design

Contributed by Enrico Macii, EIC, IEEE TCAD, enrico.macii@polito.it

TCAD receives on average 50 submissions every month. Of these, 30 are new papers and 20 are revisions. Our current backlog of papers that have been accepted but are waiting for publication is at 187 papers, equivalent to a full-year of TCAD issues. Clearly, this is an unacceptable delay for our authors whose papers have been accepted for publication. To address this delay, in the short term, the publishing societies (IEEE Circuits and Systems Society and CEDA) have agreed to invest resources to buy pages to clear this backlog. In addition, we are taking measures to control article length as well as improve our turnaround times to ensure our long-term efficient operation. If you have any suggestions, please drop a note to Enrico Macii, enrico.macii@polito.it .

IEEE Fellows Elected in 2005 in EDA

André Ivanov, University of British Columbia, for contributions to IP for system-on-chip (SoC) testing

Magdy S. Abadir, Freescale Corp., for contributions to the test and verification of microprocessors

Enrico Macii, Politecnico di Torino, for contributions to power-efficient VLSI circuits and systems

Naresh R. Shanbhag, University of Illinois at Urbana-Champaign, for development of a communication-centric design paradigm for low-power systems on a chip

Charles Alpert, IBM Austin Research Laboratory, for contributions to physical design automation of VLSI circuits

Resve Saleh, University of British Columbia, for contributions to mixed-signal integrated circuit simulation and design verification

Wolfgang Kunz, University of Kaiserslautern, for contributions to hardware verification, VLSI circuit testing, and logic synthesis

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Kartikeya Mayaram, karti@eecs.oregonstate.edu or Preeti Ranjan Panda, panda@cse.iitd.ac.in

Ramesh Harjani, University of Minnesota, for contributions to the design and CAD of analog and radio frequency circuits

Martin Wong, University of Illinois at Urbana-Champaign, for contributions to algorithmic aspects of CAD of VLSI circuits and systems

Chuan-Jin Richard Shi, University of Washington, for contributions to CAD of mixed-signal integrated circuits

Most Frequently Downloaded Articles from IEEE CEDA Publications

The most-downloaded articles from IEEE Xplore in 2005 among the *Council*'s publications cover topics from wireless sensor networks to local watermarks to Intel's innovation engine. In IEEE Transactions on CAD and IEEE Design & Test of Computers, 17 and 19 of the top 25 articles, respectively, were published in 2005-2006, indicating great topical currency. See the table below for more details.

Most-Downloaded Articles in 2005	
Article	Downloads
IEEE Design & Test of Computers	
"Dynamic Power Management in Wireless Sensor Networks," vol.18, no. 2, Mar.-Apr. 2005	1,072
"Evaluation of MEMS Capacitive Accelerometers," vol. 16, no. 4, Sept.-Oct.1999	653
"FPGA and CPLD Architectures: A Tutorial," vol. 13, no. 2, Mar.-Apr. 1996	611
"Driving the $5 Billion Innovation Engine at Intel: An Interview with Patrick P. Gelsinger, Digital Enterprise Group Senior Vice President and General Manager, Intel," vol. 22, no. 2, Mar.-Apr. 2005	551
"A methodology for architectural design of multimedia multiprocessor SoCs," vol. 22, no. 1, Jan.-Feb., 2005	539
IEEE Transactions on CAD	
"BSIM Plus: An Advanced Spice Model for Submicron MOS VLSI Circuits," vol. 13, no. 9, Sept. 1994	9,374
"A Unified Approach to Reduce SOC Test Data Volume, Scan Power and Testing Time," vol. 22, no. 3, Mar. 2003	3,989
"LPRAM: A Novel Low-Power High-Performance RAM Design with Testability and Scalability," vol. 23, no. 5, May 2004	971
"Local Watermarks: Methodology and Application to Behavioral Synthesis," vol. 22, no. 9, Sept. 2003	755
"VHDL-AMS and Verilog-AMS as Alternative Hardware Description Languages for Efficient Modeling of Multidiscipline Systems," vol. 24, no. 2, Feb. 2005	740

Upcoming CEDA Events/Dick Smith, dsmith@topher.net	
CODES+ISSS	www.esweek.org
DAC	www.dac.com
Nano-Net	www.nanonets.org
FMCAD	www.fmcad.org
ICCAD	www.iccad.com
MEMOCODE	memocode.irisa.fr
MPSoC	tima.imag.fr/mpsoc
PATMOS	www.patmos-conf.org
VLSI-SOC	tima.imag.fr/conferences/VLSI-SoC06