MAY 2009

CEDA Currents

IEEE Council on Electronic Design Automation

Elections to Chair in IEEE DATC

The Design Automation TC (DATC) is involved with the use of computer-oriented techniques in all aspects of the design process of computer & electronic systems, with particular emphasis on design languages, logic synthesis, verification techniques (including digital simulation), manufacturing interface data, graphics, and database management.

Now, we are delighted to announce the next Chair of IEEE DATC: Dr. David Kung. Please note his impressive background, which will help DATC will thrive even more under his leadership – his position statement. Dr. Kung manages a department of design automation researchers and charts the future direction of design tools research for IBM. He joined the Advanced Simulation Group in IBM Research in Yorktown Heights, N.Y. in 1986 to work on a massively parallel hardware simulation engine. Subsequently, Dr. Kung joined the Logic Synthesis group and was a contributor to IBM's BooleDozer logic synthesis system. In 1999, he became the manager of the Logic Synthesis group and led project management and technical development of Placement Driven Synthesis (PDS), IBM's physical synthesis software. He received a Bachelor of Arts degree from the University of California at Berkeley, a Master of Arts degree from Harvard University and a Ph.D. from Stanford University.

By Juan-Antonio Carballo juananto@us.ibm.com

CANDE Officers for 2008-2009

The CANDE (Computer-Aided Network DEsign) Committee is a technical activity of the IEEE Circuits and Systems Society and IEEE Council on Electronic Design Automation, which acts as a working group for electronic computer-aided design. The CANDE Committee holds a yearly workshop to discuss advanced issues relevant to the CAD community. The workshop brings together practitioners, researchers, and managers from industry and academia. To encourage long-range and open discussion, no proceedings are published and no recordings of sessions are allowed. CANDE community members take an active part in identifying topics and organizing sessions. Planning sessions for the workshop are held at DAC and ICCAD each year. Attendance at the CANDE workshop is open to all EDA/CAD professionals. Members of the CAD community are encouraged to contact the chair for more information.

CANDE has played a major role in EDA, in particular through its forward-looking annual workshop and the CANDE Predictions. In this challenging time, it is particularly important for CANDE to get together leaders from industry and academia to brainstorm the future directions and strategies for the EDA and semiconductor industry. The 2009 CANDE Workshop is planned to be held in conjunction with ICCAD.

CANDE Officers for 2008-2009

Chair: David Pan dpan@ece.utexas.edu

Secretary: Subhasish Mitra subh@stanford.edu

Treasurer: Priyank Kalla kalla@eng.utah.edu

Past Chair: Forrest Brewer forrest@ece.ucsb.edu

Publicity Chair: Lou Scheffer lou@cadence.com

Workshop Chair: Farinaz Koushanfar farinaz@rice.edu

More details will be posted at http://www.cande.net

IDESA: Effective Design at 45nm

Deep submicron design confronts designers with problems not encountered at larger feature sizes. These problems will affect all designers, digital, analogue and mixed-RF. Many of the problems can be tackled by new processing techniques, but these new processing techniques have a consequential effect on design. To successfully tape-out any design at deep submicron feature sizes, you will require an appreciation of these new problems, and rigorously apply the appropriate corrective design techniques.

The IDESA Design for Manufacturing Flow course provides early insight into these new problems and solutions. Aspects of deep submicron lithography and processing, including yield analysis and defects is covered. The course explains which new post-layout manufacturability techniques were developed, why they are needed and what the effect is on layout. You will learn to assess the importance of the different process oriented effects, and how to address them during design and layout. The

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala, jayala@fdi.ucm.es or Rajesh Gupta.

course will also address the heightened importance of Design-for-Test.

There will be a demo session on Yield analysis and hands-on sessions on lithography effects and on DFM solutions during layout. The course uses the TSMC 90nm process as a reference, but the course content is even more applicable at the 65nm and 45 nm design nodes.

The IDESA Design for Manufacturing Flow course will next be taking place:

- 12th-15th May INFN Padova, Italy
- 9th-12th June Czech Technical University, Czech Republic

These IDESA courses, along with others in the areas of Analogue, Digital and RF design can be booked via the IDESA course booking web site.

More information at http://www.idesa.rl.ac.uk/

IEEE Embedded Systems Letters (ESL) - Call For Papers

IEEE Embedded Systems Letters seeks to provide a forum for quick dissemination of research results in the domain of embedded systems with a target turn-around time of three months.

Submissions are welcome on any topic in the broad area of embedded systems and embedded software, especially but not limited to:

Architectural and micro-architectural design of embedded systems; Design automation algorithms, methods, and tools for VLSI implementations; Component modeling and component-based development methodologies; Compilation and managed runtime environments for embedded systems; OS, middleware and support systems for embedded system design; Low power design and power management; Testing, validation, and verification of embedded software; Embedded sensor networks and embedded control systems: design, analysis and application to cyber-physical systems; Embedded systems security; Applications of embedded systems and software, etc.

Submitted letters must be four pages or fewer, including all figures, tables, and references. Submissions exceeding this length will be returned without review.

Papers should use 7.875in x 10.75in (20cm x 27.30cm) trim size and the IEEE transactions two-column format in 9-pt. font. In word counts, this corresponds to roughly 2200 words. Submissions to IEEE ESL must consist of original work that has not been previously published nor is currently under review elsewhere.

Please mail manuscripts to esl-submissions@cs.ucsd.edu

Cadence Design Contest

Cadence EMEA is organizing the first full custom design contest. In this unique and innovative event the best layout designers from the top academic institutions in Europe compete for the title of "*Fastest full custom layout designer of the year*".

The rules are simple. On 20th April 2009, participants received by email the schematic of an analog block. The participant who is the first to send a DRC and LVS correct implementation of the schematic back to Cadence wins the top prize. The contest is open to any student registered in an academic program (Bachelor, Master, Phd students are welcome). The winner will be invited to CDNLive! EMEA in Munich, 18-20 May 2009 and will receive a coupon for two days of training of their choice.

The award for "Fastest full custom layout designer of the year will" be delivered during the CDNLive! EMEA conference. During the Designer Expo exhibition, the winner will demonstrate their layout skills "live" and will have the opportunity to share their best practices with the conference participants.

More information at http://www.cadence.com

Upcoming Conferences / Bill Joyner, william.joyner@src.org	
DATE	Nice (France), April 20-24, 2009
GLSVLSI	Massachusetts (USA), May 10-12, 2009
NOCS	San Diego (USA), May 10-13, 2009
MEMOCODE	Cambridge (USA), July 13-15, 2009
DAC	San Francisco (USA), July 26-31, 2009
MPSOC	Georgia (USA), August 2-7, 2009
PATMOS	Delft (Netherlands), Sept. 9-11. 2009
CODES+ISSS	Grenoble (France), Oct. 11-16, 2009
ICCAD	San Jose (USA), November 2-5, 2009
NANO-NET	Switzerland, October 18-20, 2009
FMCAD	Austin (USA), November 2009

Find us online at www.c-eda.org