June 2011

Currents

CEDA

IEEE Council on Electronic Design Automation

Call for Participation: Frontiers in Analog Circuit Synthesis and Verification

The Frontiers in Analog Circuit (FAC) Synthesis and Verification Workshop, colocated with the 23rd International Conference on Computer Aided Verification (CAV), will be held 14-15 July 2011 in Cliff Lodge, Snowbird, Utah.

While the development of digital circuits is supported by many EDA tools, the development of analog and mixed-signal (AMS) circuits has lagged behind—remaining essentially an ad hoc activity, neither facilitating reuse nor easily integrated into a system-level development process. Some of the reasons for this are inherent in the technical differences between digital and analog computation. Others are more sociological, concerning the respective communities; for example, the cultural distance between EDA software developers and analog designers is far greater than that between EDA software developers and digital designers.

With the advent of embedded SoCs, this situation puts the development of analog subsystems (necessary for all interactions with the physical world) on the critical path of new product development. The semiconductor industry now realizes it needs more advanced CAD tools for simulation, verification, test, design space exploration, model reduction, synthesis, and integration with digital subsystems.

The goal of this workshop is to bring together analog designers, EDA tool providers, and researchers from verification, simulation, and control to advance the state of the art of AMS synthesis and verification. Topics of interest include (but are not limited to) modeling approaches for analog circuits at different abstraction levels; verification of continuous models using hybrid system techniques; model checking and theorem-proving methods; use of assertions to detect errors during simulation (and for postfabrication testing); fast simulation of AMS circuits; parameter space exploration; component-based methodologies for AMS circuits; analysis of timing, power, and heat; methods that integrate verification, test, and postsilicon diagnosis; correct-by-construction approaches to AMS design, including synthesis; and analog reuse.

See http://www.async.ece.utah.edu/FAC2011 for details.

CEDA Lunch at DAC 2011

The traditional CEDA lunch will take place on 7 June 2011 during the celebration of the 48th Design Automation Conference (DAC) in San Diego, California. Dwight Hill (from Synopsys) is organizing this year's lunch.

During the lunch, Shekhar Y. Borkar (Intel Fellow at Intel Labs and director of the Microprocessor Technology Lab at Intel) will give a talk entitled "The Truths and Myths of Embedded Computing."

Computers have become ubiquitous, from powerful data centers housing supercomputing clusters to tiny microcontrollers in your toothbrush. However, the embedded-computing discipline does not get its fair share of attention. This talk will define the scope of embedded computing, compare it to general-purpose computing with appropriate metrics, challenge the myths that are floating around, and uncover the truths. The talk will also discuss challenges in architecture, design, and test of future embedded computers, which will become even more ubiquitous as they become part of general-purpose computers.

Shishpal S. Rawat, Intel, shishpal.s.rawat@intel.com

Melvin A. Breuer Wins 2011 EDAA Lifetime Achievement Award

The European Design and Automation Association (EDAA) Lifetime Achievement Award goes each year to one individual who, during his or her lifetime, has made outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems. To be eligible, candidates must have made innovative contributions that have impacted the way electronic systems are designed.

This year's award was presented to Melvin A. Breuer at the plenary session of the 2011 Design, Automation and Test in Europe (DATE) Conference, held 14-18 March in Grenoble, France. Mel Breuer can be called a "renaissance man" and an innovator in the area of CAD and testing of digital systems. He has contributed to the growth of EDA from the early days and has performed pioneering work and long-lasting results.

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es) or Rajesh Gupta.

Melvin A. Breuer is the Charles Lee Powell Professor of Electrical Engineering and Computer Science at the University of Southern California, Los Angeles. He has a PhD in electrical engineering from the University of California, Berkeley.

See http://www.edaa.com for more information.

Call for Papers for a Special Issue in Integration, The VLSI Journal

Integration, The VLSI Journal seeks papers for a Special Issue on Thermal Modeling and Simulation, Thermal-Aware Design, and Thermal Management for 2D/3D ICs. One of the major challenges to continually improving the integration density of information processing and communication systems is heat removal in ICs. This heat dissipation is caused by increased power density with every new technology generation, which is the consequence of having smaller transistors and faster clock speeds.

Moreover, new design and architecture techniques, such as 3D stacked integration and multicore processors, further exacerbate this problem. High power densities are already a major concern in 2D systems, because the excessive resulting temperature exacerbates thermal and reliability conditions. But the situation becomes more severe in 3D systems because 3D integration introduces even higher power densities, owing to the placement of computational units on top of one another. Therefore, the *International Technology Roadmap for Semiconductors* (*ITRS*) has identified thermal management and effective cooling techniques as one of five key challenges during the next decade for achieving the projected performance goals of the industry.

This special issue will cover recent progress in thermal-related design techniques for 2D multicore and emerging 3D systems such as thermal modeling, simulation, dynamic thermal management, thermal-aware physical design and optimization, and thermal-related reliability modeling and optimization techniques. Papers with in-depth, extensive coverage of the following topics are welcome: compact thermal (heat) modeling for 3D integrated SoCs; compact thermal modeling and characterization for multicore systems; fast thermal simulation and analysis for 3D and multicore systems; thermal and mechanical stress modeling and simulation; dynamic thermal management and regulation techniques for 3D and multicore systems; thermal modeling and on-chip management using active cooling techniques; thermal- and power-aware task scheduling and optimization; thermal-aware physical design and optimization (placement, floorplanning, and logic synthesis); active cooling techniques for 3D high-performance ICs; dynamic, leakage, and total power estimation techniques; and reliability analysis and optimization techniques related to negative-bias temperature instability (NBTI) or positive-bias temperature instability (PBTI).

Manuscripts are subject to peer review and should be submitted online at *http://ees.elsevier.com/vlsi* by 30 June 2011. When choosing "Article Type," please select "Special Issue Thermal IC Design." All manuscripts should conform to the standard formats indicated in the "Guide for Authors" at *http://authors.elsevier.com/journal/vlsi*.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in February 2011 were as follows:

- "Design of a Low-Cost Underwater Acoustic Modem," by B. Benson et al.
- "Minimum-Energy Operation via Error Resiliency," by R.A. Abdallah and N.R. Shanbhag
- "Control Focused Soft Error Detection for Embedded Applications," by K. Shankar and R. Lysecky
- "Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles," by C. Spelta et al.
- "Fault Classification for SRAM-Based FPGAs in the Space Environment for Fault Mitigation," by C. Bolchini and C. Sandionigi

Upcoming Conferences (Bill Joyner, william.joyner@src.org)	
DAC	San Diego, Calif., 5-10 June 2011
MEMOCODE	Cambridge, UK, 11-13 July 2011
PATMOS	Madrid, 26-29 September 2011
VLSI- SoC	Hong Kong, 3-5 October 2011
FMCAD	Austin, Texas, 30 Oct.-2 Nov. 2011
ICCAD	San Jose, Calif., 6-10 November 2011

Find us online at www.c-eda.org.

IEEE Embedded Systems Letters *is open for submissions. Visit mc.manuscriptcentral.com/les-ieee*

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es) or Rajesh Gupta.