CEDA
IEEE Council on Electronic Design Automation

CFP for IEEE Embedded Systems Letters
Special Issue on Rigorous Modeling and Analysis of Cyber-Physical Systems

Embedded microprocessors and associated hardware resources constitute more than 90% of the computing systems in use today. Many of these embedded systems are deployed in safety-critical monitoring and control applications. These systems run real-time applications that must satisfy logical correctness, timing, power, and reliability constraints. They range from traditional stand-alone systems to highly networked cyber-physical systems, spanning a diverse array of hardware and software architectures and control models.

Examples include automobile adaptive braking, industrial robotic assembly, medical pacemakers, autonomous (ground, air, and sea) vehicular travel, remote surgery, physical manipulation of nanostructures, and space exploration. Because all these embedded systems interact directly with the physical world and often impact human lives, their physical safety must be guaranteed.

Obviously, the correctness of these embedded and cyber-physical systems depends not only on the actions or results they generate but also on the time at which these actions are performed.

The goal of this special issue is to present state-of-the-art techniques and tools for the formal specification and verification of embedded systems (hardware, software, and the environment in which these systems are embedded), so that their safety and performance can be guaranteed before they are deployed on target platforms.

Topics include, but are not limited to the following, as applied to embedded and cyber-physical systems:

- design space exploration and synthesis;
- automatic optimization of specifications;
- automatic optimization of compilers and code generators;
- timing and performance analysis;
- timing analysis of functional reactive systems;
- model-based testing;
- correct-by-construction;
- requirements modeling and analysis;
- model-driven engineering;
- application of formal methods in the design and validation of embedded systems;
- safety analysis; and
- code generator verification.

Important dates for this special issue are as follows:

Manuscript due: 1 February 2013

Reviews completed: 1 April 2013

Expected publication date: 1 June 2013

For more information, please contact Guest Editors Albert M.K. Cheng (University of Houston, Texas), cheng@cs.uh.edu*; and Ramesh S. (GM Global R&D),* ramesh.s@gm.com*.*

CEDA Honors Distinguished Members of EDA Community

The IEEE Council on Electronic Design Automation (CEDA) is proud to honor two distinguished members of the EDA community: Luca Carloni (Columbia University in New York) and Joel Phillips (Cadence Research Laboratories).

Luca Carloni has won this year's Early Career Award for his seminal contributions to system-level design, including latency-insensitive design, on-chip communications synthesis, and compositional design-space exploration.

CEDA's Early Career Award honors an individual who has made innovative and substantial technical contributions to electronic design automation (EDA) in the early stages of his or her career. Contributions are evaluated according to the individual's technical merit and creativity in performing research, with consideration of his or her published record and the references accompanying the

nomination. The award is equally available to contributors from academic and industrial institutions.

Joel Phillips has won the Outstanding Service Contribution Award for his excellent work as the general chair of the 2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). He has been a member of the ICCAD Executive Committee for five years.

"Professor Carloni and Dr. Phillips have both made important contributions to EDA, and CEDA is pleased to be able to recognize both of them," noted David Yeh, director of Integrated Circuit and Systems Sciences at Semiconductor Research Corp. and chair of CEDA's Awards Committee.

Luca Carloni is an associate professor in the Department of Computer Science at Columbia University in New York. His research interests include methodologies and tools for multicore SoC platforms, with emphasis on system-level design and communication synthesis, design and optimization of networks on chips (NoCs), embedded software, and distributed embedded systems. He has a Laurea in electronics engineering from the University of Bologna in Italy; and he has an MS in engineering and a PhD in electrical engineering and computer sciences, both from the University of California at Berkeley.

Joel Phillips is a research scientist at Cadence Research Laboratories. His research interests include the development of numerically oriented algorithms for solving problems in EDA. He has a BS in physics and electrical engineering, and an MS and a PhD in electrical engineering, all from the Massachusetts Institute of Technology (MIT).

For more information on these awards, please visit www.c-eda.org.

Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in August 2012 were as follows:

- "Opal: A Multiradio Platform for High Throughput Wireless Sensor Networks," R. Jurdak et al.

- "Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles," by C. Spelta et al.

- "Fault-Tolerant Architecture for an MPEG-4 Based Video Decoder Driver," by S.P. Kamat

- "Managing Battery and Supercapacitor Resources for Real-Time Sporadic Workloads," by C.M. Krishna

- "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," by P. Razaghi and A. Gerstlauer

Upcoming Conferences (David Atienza, david.atienza@epfl.ch)	
VLSI Design	Pune, India, 5-10 January 2013
ASP-DAC	Yokohama, Japan, 22-25 January 2013
DATE	Grenoble, France, 18-22 March 2013
GLSVLSI	Paris, France, 2-4 May 2013
NOCS	Tempe, Arizona, 21-24 April 2013
DAC	Austin, Texas, 2-6 June 2013

IEEE Embedded Systems Letters **is open for submissions. Visit mc.manuscriptcentral.com/les-ieee**