



## IEEE Council on Electronic Design Automation

### ***Donald O. Pederson Best Paper Award***

Every year, the IEEE Council on Electronic Design Automation (CEDA) recognizes the best paper published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* with the Donald O. Pederson Best Paper Award. This award is based on general quality, originality, contributions, subject matter, and timeliness. Nominated articles must be published during the two calendar years preceding the award.

The winners of this year's award were Ümit Y. Ogras (Intel), Paul Bogdan (Carnegie Mellon University), and Radu Marculescu (Carnegie Mellon University) for their paper, "[An Analytical Approach for Network-on-Chip Performance Analysis](#)" (published in the December 2010 issue).

This is the first paper to present a complete analytical solution to the fundamental problem of average performance analysis in multiprocessor systems where communication occurs via the network-on-chip (NoC) approach. This solution relies on a new router model that enables deriving closed-form expressions for performance metrics such as average latency and throughput, and feedback about the network characteristics at a fine level of granularity.

Unlike previous, primarily simulation-based, approaches for NoC performance evaluation, which were slow and provided limited insight, the proposed approach is both accurate and scalable. Moreover, it can be used to obtain fast performance estimates, and hence guide the NoC design process within an optimization loop. This paper is thus a unique and outstanding contribution with potential for a strong and lasting impact.

### ***2012 Mac Van Valkenburg Award***

Giovanni De Micheli has received the 2012 Mac Van Valkenburg Award for sustained contributions to theory, practice, and experimentation on design methods and tools for integrated circuits, systems, and networks. De Micheli

has been a long-time supporter of CEDA, which he co-founded in 2005.

The Mac Van Valkenburg Award is the highest honor given by the IEEE Circuits and Systems Society (one of the member societies of CEDA) to one of its members. It honors an individual for outstanding technical contributions and distinguished leadership in a field within the scope of the IEEE Circuits and Systems Society. The award is based on the quality and significance of contribution, and continuity of technical leadership.

De Micheli is a professor and director of the Institute of Electrical Engineering at the Swiss Federal Institute of Technology Lausanne (EPFL), a Fellow of IEEE and the ACM, and a member of Academia Europaea. His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies, NoCs, and 3D integration. He is also interested in heterogeneous platform design, including electrical components and biosensors, as well as data processing of biomedical information.

De Micheli is the leader of Nano-Tera.ch, a Swiss national program supporting research in engineering of complex (terascale) systems for health, security, energy, and the environment using nanotechnologies.

Nano-Tera.ch is a partnership involving the two Swiss polytechnics (EPFL and the Swiss Federal Institute of Technology Zurich [ETHZ]), four universities (University of Neuchâtel, University of Basel, University of Geneva, and University of Italian Switzerland), and the Swiss Center for Electronics and Microtechnology (CSEM). The broad objectives of the Nano-Tera.ch program are both to improve quality of life and security of people, and to create innovative products, technologies, and manufacturing methods. Currently, the program funds 68 research projects, involving about 700 researchers and 27 industrial partners, and it supports about 120 doctoral theses.

## 2012 CEDA CAD Contest

Contests and benchmarks have recently been successful in driving research in the EDA domain forward in different areas, as witnessed by events featured at the 2012 International Symposium on Physical Design (ISPD), the 2012 ACM/IEEE International Workshop on Timing Issues (TAU), and the 2012 Design Automation Conference (DAC). To encourage better research development on timely and practical EDA problems across all domains, a new international CAD Contest is being held this year under the joint sponsorship of CEDA and the Ministry of Education of Taiwan. Three problems covering logic synthesis, physical synthesis, and physical verification (designed by industry experts from Cadence Design Systems, IBM, and Mentor Graphics) are being presented this year.

The predecessor of this contest was the annual CAD Contest in Taiwan, sponsored by the Ministry of Education, which was held for 12 consecutive years and successfully boosted EDA research momentum in Taiwan. The contest generally comprised problems contributed by EDA vendors, IC and IP design houses, and research institutes. More than 100 teams participated in the contest annually. The winning teams published their techniques and results at top journal and conference papers. Most of the winners further pursued their careers in the EDA area as faculty members, researchers, or engineers at top-tier companies.

The 2012 CAD Contest results will be announced in a special session at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), held 5-8 November 2012 in San Jose, California. This session will include three presentations from the contest organizers for the three contest problems and an award ceremony. Each contest organizer (topic chair) will present detailed information about the corresponding contest problem, including the problem description, benchmarks, and evaluation.

Along with the contest, a new set of industrial benchmarks for each contest problem will be released to facilitate evaluations of related research results. These benchmark suites are expected to play a further role in advancing related research.

Additional details about this contest are available at [http://cad\\_contest.cs.nctu.edu.tw/CAD-contest-at-ICCAD2012](http://cad_contest.cs.nctu.edu.tw/CAD-contest-at-ICCAD2012).

## Papers in IEEE Embedded Systems Letters

The top-five accessed articles from *IEEE Embedded Systems Letters* in June 2012 were as follows:

- “[Cross-Layer Optimizations in Solid-State Drives](#),” J.-H. Wang, H.-H. Chen, W.-J. Su, and D.-W. Chang
- “[Opal: A Multiradio Platform for High Throughput Wireless Sensor Networks](#),” by R. Jurdak, K. Klues, B. Kusy, C. Richter, K. Langendoen, and M. Brunig
- “[Smartphone-Based Vehicle-to-Driver/Environment Interaction System for Motorcycles](#)” by C. Spelta, V. Manzoni, A. Corti, A. Goggi, and S.M. Savaresi
- “[Coroutine-Based Synthesis of Efficient Embedded Software from SystemC Models](#),” by W. Liu, J. Xu, J.K. Muppala, W. Zhang, X. Wu, and Y. Ye
- “[Fault-Tolerant Architecture for an MPEG-4 Based Video Decoder Driver](#),” by S.P. Kamat

Upcoming Conferences (David Atienza, <a href="mailto:david.atienza@epfl.ch">david.atienza@epfl.ch</a> )	
FMCAD	Cambridge, UK, 22-25 October 2012
ICCAD	San Jose, Calif., 5-8 November 2012
ASP-DAC	Yokohama, Japan, 22-25 January 2013

IEEE Embedded Systems Letters *is open for submissions*. Visit [mc.manuscriptcentral.com/les-ieee](http://mc.manuscriptcentral.com/les-ieee)

### IEEE COUNCIL ON ELECTRONIC DESIGN AUTOMATION

President: DONATELLA SCIUTO President-Elect: SANI NASSIF Past President: ANDREAS KUEHLMANN

Secretary: YAO-WEN CHANG VP Conferences: DAVID ATIENZA VP Finance: SHISHPAL RAWAT

VP Publications: SACHIN SAPATNEKAR VP Publicity: RAJESH GUPTA

VP Strategy: WILLIAM JOYNER VP Activities: JOEL PHILLIPS

CEDA Currents is a publication of IEEE CEDA. Please send contributions to Jose L. Ayala ([jayala@fdi.ucm.es](mailto:jayala@fdi.ucm.es)).

© 2012 IEEE. All rights reserved.