April 2021 Currents

CEDA
IEEE Council on Electronic Design Automation

Join the Conversation on LinkedIn!

We are excited to announce the launch of a new CEDA LinkedIn Company Page. The CEDA LinkedIn Group Page will remain in place for members to communicate with one another in a closed setting, while the LinkedIn Company Page will serve as a place to find official updates and communications from the Council. The new page will allow members to add CEDA as a volunteer position on their LinkedIn profile and tag the Council in posts.

CAD for Assurance Panel: Microelectronics Assurance Under Zero Trust Model

IEEE CEDA's Hardware Security and Trust Technical Committee (HSTTC) developed the "CAD for Assurance" website and tools for faculty, students, post docs, and practitioners in the hardware security community to disseminate their work. This initiative also includes a series of monthly, virtual webinars.

The next webinar in this series is a panel on Microelectronics Assurance Under Zero Trust Model on 19 April at 11:00 AM-12:20 PM ET. The webinar will be moderated by Saverio Fazzari and feature panelists Rob Aitken, Brian Dupaix, Matt French, and James Wilson.

Registration is required. For more information on this webinar series and to register, visit the CEDA website.

Call for Papers: IEEE Embedded Systems Letters Special Issue "Hardware Security for Post-CMOS Technologies"

IEEE Embedded Systems Letters seeks to provide a forum of quick dissemination of research results in the domain of embedded systems with a target turnaround time of no more than three months. The journal is currently published quarterly and consists of new, short and critically refereed technical papers. This special issue is about attacks and defenses of the emerging technology based embedded systems; and covers several aspects ranging from technology, circuits, architecture, automation and vulnerability investigations.

Modern societies are heavily dependent on electronic systems. Especially with the emergence of IoT and advanced embedded electronic devices, such as mobile computers, wearables, and smartwatches, personalization is apparent. The rise of the electronic device jungle has provided a large attack surface to the bad actors to manipulate hardware and information processed. The attacks can significantly affect the three foundational aspects of secure hardware: confidentiality, integrity, and availability. Those cornerstones of hardware security in embedded systems are in danger of physical and remote attacks by adversaries during different periods of their design and life cycles.

Depending on the attack, the countermeasure can also be innovative and wide in range. The future of computing is expected to be in the nano-structures composed of different types of devices and emerging technologies such as ReRAMs, biosensors, MRAM, and others. In this special issue, we cover attacks and countermeasures in future-generation embedded systems that utilize their nano-structure composition for security.

Submissions are due 30 July. The call for papers can be downloaded here.

Call for Papers: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits Special Issue "Monolithic 3D Integration for Energy-Efficient Computing"

As the traditional 2D scaling is approaching its physical limit, there is a great motivation to explore the 3rd dimension for future integrated circuit design. The Memory industry has already adopted monolithic 3D integration (e.g. in 176-layer 3D NAND Flash), while the 3D vertical integration structure of logic transistors (e.g. 3D stacked nanosheets, NMOS on top of PMOS) is emerging for sub-3 nm logic nodes. The other trend is to stack the embedded non-volatile memories (e.g. RRAM, PCM, MRAM, FeFET) on top of CMOS using the back-end-of-line (BEOL) processing.

Taking one step further, integration of multiple tiers of active transistors with embedded memories is expected to offer significant improvements of the throughput and energy efficiency thanks to the massive connectivity between logic and memories. Besides the technological breakthroughs, circuit design automation methodologies become key enablers to optimize the tier partitioning in monolithic 3D architectures. In addition, heat dissipation

should be taken care of by accurate thermal modeling in these monolithic 3D architectures. New heat spreading materials and advanced embedded cooling techniques are also important.

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of monolithic 3D integration technologies.

Submissions are due 15 April. The call for papers can be downloaded here.

DAC 2021 New Dates Announced

The Design Automation Conference (DAC) is the premier event devoted to the design and design automation of electronic systems and circuits. DAC focuses on the latest methodologies and technology advancements in electronic design. The 58th DAC will bring together researchers, designers, practitioners, tool developers, students and vendors.

In anticipation of potential travel restrictions and continuing state and local restrictions on large public gatherings, the DAC Executive Committee along with the event sponsors, ACM and IEEE have decided to postpone the dates of the conference and exhibition until later in the year to provide more time for vaccination distribution and the implementation of additional health and safety practices.

DAC 2021 will be hosted in San Francisco, California, USA on 5-9 December 2021. For more information, visit the DAC website.

ICCAD 2021 Has Gone Virtual

ICCAD is the premier conference devoted to technical innovations in Electronic Design Automation. Original technical submissions on, but not limited to, the following topics are invited: System-level CAD, Synthesis, Verification, Physical Design, Analysis, Simulation, and Modelling, and CAD for Emerging Technologies, Paradigms.

Due to the ongoing global events, the Organizing Committee has moved ICCAD 2021 to a hybrid format with the technical program in virtual format on 1-4 November and an in-person networking event on 5 November. Abstract submissions are due 21 May.

For more information on ICCAD 2021, visit the conference website.

2020 Outstanding Service Award

The CEDA Outstanding Service Award is presented to volunteers, specifically those who served as former General Chairs of a major CEDA conference, for their exceptional commitment and service to the EDA community.

We thank the following for their service to the EDA community in 2020:

- Kwang-Ting Tim Cheng, ASP-DAC
- Huazhong Yang, ASP-DAC
- Giorgio Di Natale, DATE
- Tulika Mitra, ESWEEK
- Yuan Xie, ICCAD
- Zhou Li, DAC

Recipients received an engraved plaque and are recognized at their choice of CEDA sponsored conference in the year following their year of service. See a full list of CEDA OSA recipients on the website.

Find us online at **ieee-ceda.org**
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Please send contributions to Vasilis F. Pavlidis

Contributions Form

IEEE Embedded Systems Letters is open for submissions

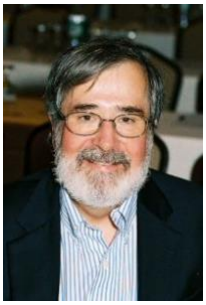
Visit http://bit.ly/ESLSubmissions

IEEE Design & Test is open for submissions

Visit http://bit.ly/DTSubmissions

Professor Edmund M. Clarke

1945 –2020



Dear EDA community,

We sincerely hope that everyone is well and staying healthy in this unprecedented time. It is our great regret to inform that Professor Edmund M. Clarke, a professor emeritus at Carnegie Mellon University, died of COVID-19 after a long illness in December 2020. He was 75. As you all know, Professor is best known for his work in model checking, an automated method for formally verifying computer systems and won the prestigious A.M. Turing award thanks to his seminal contributions to our fields. Here are a few paragraphs of eulogies from ones who know Prof. Clarke well.

--by Randal E. Bryant, the Founders University Professor of Computer Science Emeritus at Carnegie Mellon University: Ed Clarke's work on model checking has had a major impact on the use of formal verification in EDA. Model checking enables users to describe desired properties of a finite-state system (e.g., a sequential circuit) and then automatically determine whether or not a system satisfies that property. Ed (along with his PhD student Allen Emerson) formulated model checking in the early 1980s, but it could only handle very small systems. It first became viable for real-life systems with the advent of BDD-based symbolic model checking in the mid-1990s, initially through the efforts of Ed's PhD student Ken McMillan. Then in the late 1990s, Ed, along with a group of PhD students and post-docs, formulated bounded model checking. This can only prove that desired properties would hold up to some fixed number of cycles, but it leverages Boolean satisfiability (SAT) technology to scale to much larger systems. Over the past four decades, these ideas have been revised and refined by Ed, his students and post-docs, as well as researchers around the world to make model checking one of the cornerstones of formal verification. Ed was a rare example of someone who could build on his theoretical background in formal logic, while also having a practical mind and an appreciation for addressing the needs of real-life system designers. He was especially gifted at mentoring his PhD students and his post-docs, many of whom have pursued successful careers in EDA, both in academia and in industry.

--by Ken McMillan, a former graduate student: Ed was a founder and visionary leader in the field of Computer-Aided Verification. His early work on Temporal Logic Model Checking with Alan Emerson in the 1980's set the paradigm for a field that continues to be vibrant and active. Over a period of decades, he and his research group were deeply involved in nearly all of the major research advances that led to the practical use of model checking in industry, including the applications of Decision Diagrams and Boolean Satisfiability, and the development of automated abstraction. He was also a friend, a mentor and an inspiration to many in the field, including myself. As his graduate student in the late 1980's, I experienced the exciting atmosphere of possibility in the new research area that Ed was instrumental in creating. His style of advising students was subtle, and yet surprisingly effective. He would observe his student's work, make unexpected connections from his broad knowledge, and suggest readings from the many alphabetized stacks of papers he kept in his office, always somehow pushing the student in the right direction. I think this light touch contributed to the remarkable impact of his research group over the years. Ed's ideas, his enthusiasm and his generosity of spirit have touched the lives of generations of researchers and provided a foundation for many successful careers. His vision will continue to inspire generations to come.

–by Dr. Andreas Kuehlmann, the CEO of Tortuga Logic, Inc.: Professor Ed Clarke's impact on us cannot be overstated. His foundational contributions to formal verification changed the way we think about systems and how to ensure their correctness. It led to many theoretical and practical results with broad influence on industry's best practices and triggered much subsequent research. Ed inspired all of us to tackle problems with a combination of rigorous thinking and seeking solutions that are practical. He mentored many graduate students who themselves became leaders in their respective fields and will continue to carry his vision forward. I was very fortunate to work with Ed and many of his students over the years. I am sure I speak for many in saying that he will be missed.

We lost a giant in our EDA field, but his works and contributions will be remembered for a long time.

Sincerely,

Yao-Wen Chang,
The President of IEEE CEDA