August 2021 CEDA Currents
IEEE Council on Electronic Design Automation

Call for Participation: 2021 Design Automation Conference (DAC)

DAC is the premier event devoted to the design and design automation of electronic systems and circuits. DAC focuses on the latest methodologies and technology advancements in electronic design. The 58th DAC will bring together researchers, designers, practitioners, tool developers, students and vendors.

The 2021 DAC program can be found here. Registration for Research Paper Authors is now open. Early registration with reduced rates opens September 7 and will go through November 20. Registration rates can be found here.

Registration is now open for HACK@DAC, a hardware security challenge contest that begins October 4. For more information and to register, visit the DAC website.

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for Ph.D. students to present and discuss their dissertation research with people in the EDA community. The deadline to submit abstracts has been extended to August 31. Notifications will be sent September 30. View the call for papers for submission guidelines, important dates, and more information.

Call for Nominations: CEDA Distinguished Lecturer Program Class of 2022-2023

CEDA invites nominations for its Distinguished Lecturer Program Class of 2022-2023. The DL Program is the outreach program of CEDA that brings distinguished speakers from academia and industry to give presentations to CEDA chapters, events, and industries in a variety of venues and formats.

Nominees must meet the following criteria:

- The nominee must be nominated by a CEDA participant who does not have a conflict with the selection process.
- No self-nomination is allowed.
- If you are looking for a nominator, we encourage you to contact the chair of your corresponding CEDA local chapter.
- The DL nominee must be a well-recognized expert in their field because of their research, teaching, service activities, and an inspiring speaker.

Send all questions to the CEDA DLP Manager, Mehdi Tahoori. Please complete the form to nominate a deserving colleague.

Call for Participation: CEDA Virtual Distinguished Lecturer Webinar Series

The Virtual Distinguished Lecturer Program allows us to continue to serve the CEDA participants and the electronic design automation community by giving them the opportunity to hear from our respected Distinguished Lecturers.

Dr. X. Sharon Hu (University of Notre Dame) will present "In-Memory Computing with Associative Memories — A Cross-Layer Perspective" on August 19 at 11:00 AM – 12:00 PM ET. Registration is free but required via Zoom.

About the Talk: Sharon will present a showcase of several representatives cross-layer AM based design efforts. In particular, she will highlight how different non-volatile memory technologies (such as RRAM, FeFET memory and Flash) can be exploited to implement various types of AM (e.g., exact and approximate match, ternary and multi-bit data representation, and different distance functions). Sharon will use several popular machine learning and security applications to demonstrate how they can profit from these different AM designs. End-to-end (from device to application) evaluations will be analyzed to reveal the benefits contributed by each design layer, which can serve as guides for future research efforts.

Visit the website for a full listing of upcoming webinars.

Call for Nominations: TCAD and D&T EiCs

The IEEE Council on Design Automation (CEDA) invites nominations for the position of Editor-in-Chief (EiC) for the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) and IEEE Design&Test (D&T). Self-nominations are permitted.

The TCAD EiC term of duty begins January 1, 2022 and ends December 31, 2023. The D&T EiC term of duty begins on January 1, 2022 and ends December 31, 2024.

Nominations should be submitted by September 5 to ensure full consideration. Visit the website for more information and to submit a nomination form.

CAD for Assurance Webinar: Malware Detectors and Introduction to Common Evaluation Platform (CEP)

IEEE CEDA's Hardware Security and Trust Technical Committee (HSTTC) developed the "CAD for Assurance" website and tools for faculty, students, post docs, and

practitioners in the hardware security community to disseminate their work. This initiative also includes a series of monthly, virtual webinars.

The next webinar is August 13 at 11:00 AM-12:20 PM ET. Kanad Basu (UT Dallas) will present Malware Detectors. Brendon Chetwynd (MIT Lincoln Lab) will present Introduction to Common Evaluation Platform (CEP).

Registration is required. For more information on this webinar series and to register, visit the CEDA website.

Call for Papers: IEEE Embedded Systems Letters Special Issue

The Special Issue on Reliable and Resilient Digital Manufacturing is about digital manufacturing that is enabled by embedded processors, cyber-physical systems (CPS) and IoT devices.

The special issue covers several aspects ranging from security and privacy of digital manufacturing systems, to resilience metrics, computer-aided design innovations and reliability issues. Submitted papers to the special issue must conform to the technical requirements of ESL.

Note for this special issue a 3-minute video preview will be required later for accepted papers. The deadline to submit is September 10, 2021.

For a full list of topics, important dates, and guest editors, visit our website.

Call for Papers: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits Special Issue

The Special Issue on Cryogenic Semiconductor Devices and Circuits for Computing is on emerging cryogenic semiconductor devices and circuits for high performance computation.

The focus and emphasis of these special topic papers is beyond Josephson junctions-based devices and circuits; such as single flux quantum (SFQ), etc. Some example topics of interest include cryogenic memories, short-range and long-range connectivity in the devices and circuits, etc. Papers are encouraged that address new emerging functionality at cryogenic temperatures at all levels (materials, device, circuits, and systems), including showing at a system level how such advanced functions can be useful for computing tasks and understanding the system-level energy efficiency and speed.

The deadline to submit is October 1, 2021. For a full list of topics, submission guidelines, and dates download the CFP.

Call for Participation: SLIP 2021 Workshop

The 2021 ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP) is the 23rd edition of the Workshop and will be hosted virtuallyl on November 4, 2021. SLIP, co-hosted with ICCAD 2021, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology.

There are two special sessions this year: 3DIC Architectures and High-Speed, Energy-Efficient On/Off-Chip Interconnects; and DTCO-Enhanced Physical Design and EDA Flows.

The deadlines to submit abstracts and papers are August 8 and August 15, 2021, respectively. For a full list of topics, submission guidelines, and more, visit the SLIP website.

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Please send contributions to Vasilis F. Pavlidis

Contributions Form

IEEE Embedded Systems Letters is open for submissions

Visit http://bit.ly/ESLSubmissions

IEEE Design & Test is open for submissions

Visit http://bit.ly/DTSubmissions