A call for papers is now open for the *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* special topic on "Energy-Efficient Compute-in-Memory with Emerging Devices".

Aims and Scope

Deep neural networks (DNNs) have shown extraordinary performance in recent years for various applications including image classification, object detection, speech recognition, natural language processing, etc. Accuracy-driven DNN architectures tend to increase the model sizes and computations at a very fast pace, demanding a massive amount of hardware resources. Frequent communication between the processing engine and the on-/off-chip memory leads to high energy consumption, which becomes a bottleneck for the conventional DNN accelerator design.

To overcome such challenges, compute-in-memory (CIM) has been proposed as a promising scheme for energy-efficient DNN acceleration. The weights are stored in the memory cells and the multiply-and-accumulate (MAC) operation is performed within the memory array by asserting multiple rows simultaneously. Regarding the memory technologies for the CIM scheme, SRAM is mature but is volatile, consumes large area (e.g. 8T/10T bitcells) and suffers from the leakage power in the CMOS devices. Such disadvantages promoted the non-volatile memory (NVM) as an attractive solution for area-efficient CIM-based DNN acceleration.

NVMs presented in the literature from both academia and industry include resistive random access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic random access memory (STT-MRAM) and ferroelectric field effect transistor (FeFET). Notably, the industry has been heavily investing in the commercialization of NVM technologies, e.g. TSMC's 40nm RRAM, Intel's 22nm RRAM, TSMC's 40nm PCM, Intel's 22nm STT-MRAM, Samsung's 28 nm STT-MRAM, and Globalfoundries' 22nm FeFET.

Compared to SRAM-based CIM, NVM based CIM could provide bitcell array density benefits, but the peripheral circuits need to be considered together, and achieving higher energy-efficiency can be challenging due to high current consumption when turning on multiple low-resistance-state devices simultaneously. To address these concerns, new schemes for energy-efficient CIM with emerging NVM devices are being investigated and developed.

This special topic of the IEEE Journal on Exploratory Computational Devices and Circuits (JXCDC) is in line with such efforts and aims to call for paper submissions on the recent research advances in the area of the energy-efficient compute-in-memory spanning devices, circuits, and systems. Papers on the interaction and co-optimization of the materials and devices as well as circuits and architecture are solicited.

Topics of Interest include but are not limited to:

Prospective authors are invited to submit original works and/or extended works based on conference presentations on various aspects of compute-in-memory. Memory technologies of interest include (but not limited to) SRAM, DRAM, eDRAM, NOR/NAND Flash, and emerging NVM devices such as PCM, RRAM/CBRAM, STT-MRAM/SOT-MRAM (or other spintronic memories), FeFET (or other ferroelectric memories), etc. The following topics are specifically solicited:

- New materials and devices that can enable energy-efficient compute-in-memory
- Integration of emerging technologies with silicon for energy-efficient compute-in-memory

- Crossbar array design and array-level demonstration for energy-efficient compute-in-memory
- Peripheral circuit design for energy-efficient compute-in-memory
- Architectural-level design for energy-efficient compute-in-memory
- Algorithms and hardware co-design for energy-efficient compute-in-memory
- Benchmarking simulators for energy-efficient compute-in-memory
- New applications for energy-efficient compute-in-memory beyond deep learning (e.g. combinatorial optimization, general purpose computing, etc.)

Important Dates

Open for Submission: May 15, 2022
Submission Deadline: July 15, 2022
First Notification: August 15, 2022
Revision Submission: September 1, 2022
Final Decision: September **15**, 2022
Publication Online: October 1, 2022

Submission Guidelines

The IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC) IS AN OPEN ACCESS ONLY PUBLICATION: Charge for Authors: $1,850 USD per paper with the following discounts:

IEEE Members receive a 5% discount.
IEEE Society Members receive a 20% discount.
These discounts cannot be combined.

Paper submissions must be done through the ScholarOne Manuscripts website:
https://mc.manuscriptcentral.com/jxcdc

Guidelines for papers and supplementary materials, as well as a paper template, are provided at this website.

Inquiries for the JxCDC Journal should be sent to: JXCDC@IEEE.ORG

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