Compiler Frameworks and Co-design Methodologies for Heterogeneous Systems-on-Chip

This special issue aims to provide the targeted readers with the new advances and challenges in the area of compiler frameworks, hardware/software methodologies, and related tools to aid the design of complex heterogeneous systems.

To face the new challenges of the post-Moore era, the industry started moving from IC scaling to system scaling, introducing heterogeneous architectures as a strategy to limit the cost per function and boost energy efficiency. Nowadays, the increasing demand for performance and energy efficiency has motivated the adoption of heterogeneous platforms in several computing domains, from high-performance computing (HPC) to embedded systems. Heterogeneous systems-on-chip combine diverse processing elements, such as general-purpose processors (GPP), graphics processor units (GPU), digital signal processors (DSP), field-programmable gate arrays (FPGA), and many application-specific hardware accelerators. The real challenge of heterogeneous computing consists of identifying application tasks that can benefit from appropriate optimizations and selecting the best target processing units for those tasks. In real use cases, the programming complexity required to orchestrate task distribution may raise a significant barrier to the widespread adoption of heterogeneous architectures. Another major challenge is to ensure software portability across the growing variety of heterogeneous architectures.

Considering the described scenario, to fully exploit the power of these platforms and overcome the limits of conventional architectures, system and application designers need new tools and methodologies to address the increasing hardware/software complexity and achieve high productivity. In recent years, driven by the great momentum of domain-specific architectures (e.g., machine learning accelerators), compiler infrastructures and co-design frameworks for heterogeneous computing have represented an attractive topic for many scientific publications. The current efforts in the research area of compilation toolchains aim at facilitating the code optimization at different levels of abstraction, promoting approaches based on hardware/software co-design in diverse application domains. In the context of end-to-end frameworks, the introduction of specialized hardware units is pushing for the adoption of new methodologies (e.g., mixed-precision techniques) that make even more challenging the full exploitation of available resources.

Relevant topics for this call include, but are not limited to, the following:

- Compiler frameworks and co-design workflows for heterogeneous hardware
- End-to-end frameworks targeting heterogeneous specialized units
- Application-specific co-design methodologies for heterogeneous platforms
- Synergistic HW/SW techniques to promote parallelism in heterogeneous computing
- Novel programming paradigms to promote heterogeneous design
- Source-to-source translation and (semi-)automatic code generation for heterogeneous architectures
- Methodologies to improve software portability across heterogeneous targets

GUEST EDITORS

Luca Benini holds the chair of the Digital Circuits and Systems Group at the Integrated Systems Laboratory, ETH Zurich and is Full Professor at the Università di Bologna. He has been a visiting professor at Stanford University, IMEC, and EPFL. He served as chief architect in STMicroelectronics France. Dr. Benini's research interests are in energy-efficient parallel computing systems, smart sensing micro-systems and machine learning hardware. He has published more than 1000 peer-reviewed papers and five books. He is a Fellow of the IEEE, of the ACM and a member of the Academia Europaea. He is the recipient of the 2016 IEEE CAS Mac Van Valkenburg award and of the 2019 IEEE TCAD Donald O. Pederson Best Paper Award.

Luca Carloni is Professor of Computer Science at Columbia University in the City of New York where he leads the System-Level Design group. His research interests include methodologies and tools for system-on-chip platforms with emphasis on heterogeneous computing, design of networks-on-chip, embedded software, and distributed embedded systems. Luca co-authored over one hundred and fifty refereed papers and two patents. He received the Faculty Early Career Development (CAREER) Award from the National Science Foundation in 2006, was selected as an Alfred P. Sloan Research Fellow in 2008, and received the ONR Young Investigator Award and the IEEE CEDA Early Career Award in 2010 and 2012, respectively. Luca is an IEEE Fellow.

Giuseppe Tagliavini is an assistant professor with the Department of Computer Science and Engineering (DISI) of the University of Bologna. His main research interests are centered on parallel programming models and emerging computing paradigms, with a strong focus on ultra-low-power embedded systems. His expertise in this research field covers multiple design levels and includes optimization of applications and runtime libraries, extensions of programming languages at front-end level, code optimization in compilation toolchains, HW/SW co-design of processing units. He has published over 30 papers in peer-reviewed international journals and conferences. He is a member of ACM and IEEE technical societies.

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PROPOSED TIMELINE

- Submission Deadline: November 15, 2020
- Reviews Completed: January 15, 2021
- Major Revisions Due: February 15, 2021
- Reviews of Revisions Completed: March 15, 2021
- Notification of Final Acceptance: March 31, 2021
- Publication Materials for Final Manuscripts Due: April 10, 2021
- Publication: May 2021